# NEW SINGLE ELEMENT MEMORY TRANSISTOR WITH A PHASE TRANSITION THIN FILM MATERIAL AS A GATE INSULATOR

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# NEW SINGLE ELEMENT MEMORY TRANSISTOR WITH A PHASE TRANSITION THIN FILM MATERIAL AS A GATE INSULATOR

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A new single element phase transition memory with a gate insulator composed of a phase transition film and two silicon dioxide layers is proposed. A phase transition thin film is placed between silicon dioxide layers and hence the gate stack of the transistor has a metal-insulator-phase transition material-insulator-semiconductor (MIPIS) structure. In my experiments, Vanadium Dioxide ($VO_2$), Germanium Antimony Telluride (GST) and Samarium Nickelate ($SmNiO_3$) are employed as intermediate gate insulators, and bulk-type and suspended channel device structures are implemented. These materials go through structural phase transition with the increase of temperature and their physical properties, such as resistance, reflectance and permittivity, change drastically. The original proposition is that Joule heat induced by current flowing through the channel leads to the phase transition of a material and thus modulates the threshold voltage of a memory transistor. Polarization effect, however, dominates over the phase transition effect in fabricated devices. The counterclockwise voltage hysteresis of gate capacitance is observed in response to the gate voltage and consistent with the hysteretic behavior resulting from polarization switching. In $VO_2$ bulk-type devices, memory window of ~1 V is obtained in -4 to 4 V gate voltage cycling. Its remnant polarization of ~0.53 $\mu C/cm^2$ and coercive field of ~450 kV/cm are extracted from the saturation behavior of threshold voltage shift. Similar to other ferroelectric memory structures, the depolarization field exists. The

state of memory devices decays gradually and retention times of approximately 15 minutes are obtained at room temperature. Assuming the second order ferroelectric phase transition, the Curie-Weiss temperature of $VO_2$ is extrapolated and its value is around 450 K. At lower temperatures, the polarization of $VO_2$ disappears due to the freezing of switchable polarization. In GST suspended channel devices, hysteresis memory window of ~1 V under ±4 V cycling and retention times of hundreds of seconds are obtained. Extracted remnant polarization is ~0.13 $\mu C/cm^2$. The degradation of the polarization and charge trapping effect are observed at low temperature. In SNO bulk-type devices, space charge polarization is dominant given the fact that the response time of polarization is above 1 μs. Hysteretic behaviors induced by the space charge polarization are explained by Poole-Frenkel charge trapping/detrapping mechanism. The stored information decays gradually with the retention time of the order of ten seconds at room temperature.

# BIOGRAPHICAL SKETCH

Sang Hyeon Lee was born in Korea in 1971. He received the B.S. degree in physics from Seoul National University, Seoul, Korea, in 1998. He joined Semiconductor R&D Center in Samsung Electronics right after graduation. He was involved in the development of several DRAMs ranging from 64 Mb to 4 Gb densities. The technology nodes of DRAM devices of which he took part in the development varied from 50nm to 150nm. In 2006, he won a Samsung Fellowship for Ph.D. study including financial support and he joined the MS/Ph.D. program in Electrical and Computer Engineering at Cornell University in 2007. He performed his research under the guidance of Prof. Sandip Tiwari. He received the M.S. and Ph.D. degrees in 2011 and 2012 respectively. His Ph.D. work included a memory device design using a phase transition material, nanofabrication, characterization and analysis of memory devices, and nanoscale silicon MOSFETs. He is interested in semiconductor device physics, device characterization techniques, novel memory devices and nanofabrication technology.

To my family, friends and teachers

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# Chapter 1

# INTRODUCTION

## *1.1 Next Generation Memory*

In 1969, the history of semiconductor memory began with the introduction of a 64-bit bipolar random-access memory (RAM) used in the cache memory of an IBM computer. [1] One year later, a 1024-bit MOS dynamic RAM (DRAM) was made by Honeywell and Intel and gave a turning point to the semiconductor industry since it could store large amount of information on a single chip for the first time [2], [3]. Now after 40 years, the bit density increases ten million times and the speed increases a hundred times, which is the most remarkable progress compared to any other things in the history of mankind. Semiconductor memory has thus made an enormous progress so far and has been a front runner to contribute to the revolutionary growth of digital electronics. These days, owing to the explosive expansion of mobile market, memory has been of interest much more than before.

Semiconductor memory is classified into two types or categories according to data retention characteristics: volatile memory such as static RAM (SRAM) and DRAM, and non-volatile memory such as read-only memory (ROM), magneto-resistive RAM (MRAM), and Flash memory. Volatile memory cannot maintain the stored information without power supply and hence is used as a temporary memory. Non-volatile memory can retain the stored information even without power supply. Nonetheless, non-volatile memory is normally used as a secondary memory since it

has poor performance compared to volatile memory. As is well known, DRAM and Flash memory are the representatives of volatile and non-volatile memories, respectively. According to the memory market trend presented by iSuppli, the market share of DRAM and Flash memory exceeds 90% of total [4], which is a huge amount compared to any other products' market. Absolutely, in the memory market, DRAM and Flash memory are dominant. However, they have their own advantages and disadvantages as shown in Figure 1.1. For example, DRAM has a storage capacitor with a finite leakage current and thus it cannot keep its memory state. So, it needs to refresh its data periodically and then it has more power consumption. Moreover, its cell consists of 1 transistor and 1 capacitance (1T1C), so it has bigger cell area. Meanwhile, Flash memory has slow write and erase times and limited write endurance. Its high operation voltage is another limiting factor to be scaled down. Therefore, the driving force to develop next generation memory is making a new memory with both merits of DRAM and Flash memory.

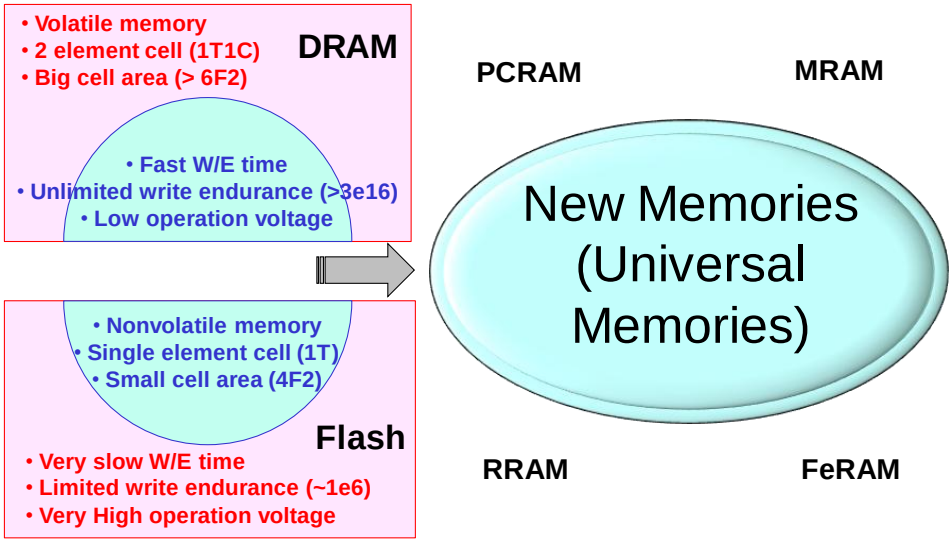



**Figure 1.1** Features of DRAM and Flash memory and examples of new memories.

Among many types of new memories, phase-change RAM (PCRAM) is the most advanced one. Samsung made a 512Mb product of PCRAM in 2010. But, it is not a main stream memory, but a memory in a niche market. Recently, nanowire or nanocrystal PCRAM has been studied [5]–[7]. Second one is MRAM. Everspin made a 16Mb product of MRAM using MTJ technology. Now, most research has been focused on spin-transfer torque MRAM [8]. Especially, in the academic field, Resistive RAM (RRAM) is the most famous one, because its fundamental physics has not been fully understood yet. There are many types of RRAM [9]: metal oxide memory, nanoconductive bridge or solid electrolyte memory, polymer (with metal nanoparticle) memory and molecular memory, etc. Ferroelectric RAM (FeRAM) had a 1T1C cell structure like DRAM in the beginning. Ferroelectric materials were used as an insulator of capacitor. On the other hand, FeFET memory with a 1T cell was suggested as universal memory, because it has a single element cell, fast transition time, and low power consumption [10]–[12]. However, due to the fundamental issue of depolarization field, it is a volatile memory and thus is considered to be an alternative to DRAM [13], [14].

For non-volatile memories at nanoscale, commercial and major research efforts have followed two paths in the last decade. The first is use of charge injection and trapping within an insulator stack that is sensed by integrating into a field effect transistor [15]. The second is use of phase change between amorphous and crystalline phase that results in conductivity change [16]. This structure employs an access element (a diode, FET, or a bipolar transistor) in series. The first approach leads to a compact design of a single element device such as the NAND architecture, but

encounters the degradation of dielectric property due to carriers' energy leading to the increase of defects during the usage. In ultra-small devices, the injection phenomena and the energetic interactions affect the reliability, endurance, and operating characteristics. Stochastic and small-scale effects continue to become increasingly dominant. The second approach employs thermally-driven phase change, and requires high current flow and power dissipation. The amorphization and crystallization processes typically happen or are initiated in the vicinity of a metal electrode. This approach encounters problems related to power, timing, and scaling issues due to surface effects and the need of area for two elements.

In my thesis, a new form of memory based on phase transition in a single element is presented conceptually. The new approach utilizes the phase transition coupled with the transistor channel and dissipated thermal energy. Information can be stored by changing other characteristics of the material – such as permittivity or conductivity without resorting to any charge transport to a memory node. Phase transitions due to correlated electrons is a collective effect in which the electron-crystal interactions lead to properties that undergo large rapid changes (phase transitions) under the influence of field, temperature, pressure, etc. Phase transition behavior in perovskite-structure cuprate compounds was used by D. M. Newns et al. to demonstrate a device, a Mott transistor, in which metal-insulator transition was employed for transistor channel creation [17]. The proposed device is a single element phase transition memory and it would operate at low bias and low power dissipation conditions, and be compatible with conventional silicon electronics. An interest in a universal memory having DRAM and Flash's merits has driven the invention of many

structures of novel memory devices and various combinations/mixtures of materials [18]. This phase transition memory may be capable of serving this area.

## *1.2 Electronic Polarization and Ferroelectric Memory*

Dielectric property is determined by the polarization of a material under an electric field. There are several types of polarization [19]: electronic polarization ($P_{el}$) induced by the displacement of electronic charges (nuclei and electrons), ionic polarization ($P_{ion}$) induced by the displacement of ionic charges (cations and anions), dipolar or orientational polarization ($P_{dip}$) induced by the alignment of permanent dipoles, and space charge or diffusional polarization ($P_{sc}$) induced by the separation of mobile charges, the hopping of trapped charges or grain coupling. The total polarization is the sum of every polarization as follows.

$$\overrightarrow{P_{tot}} = \overrightarrow{P_{el}} + \overrightarrow{P_{ion}} + \overrightarrow{P_{dip}} + \overrightarrow{P_{sc}} . \tag{1.1}$$

Each polarization has different response time and different dependence on the frequency of the electric field as shown in Figure 1.2. When the excitation frequency exceeds the relaxation frequency, dipoles cannot respond to the electric field and will not contribute to the permittivity. Therefore, each polarization has a typical frequency bandwidth responding to the electric field. For example, the response time of space charge polarization is above microsecond and hence the dielectric constant of a space charge dominant material changes gradually with sub-megahertz frequency bandwidth. So, one can infer the dominant polarization in a dielectric material by determining its dependence on the frequency of the applied electric field. In this thesis, the dielectric

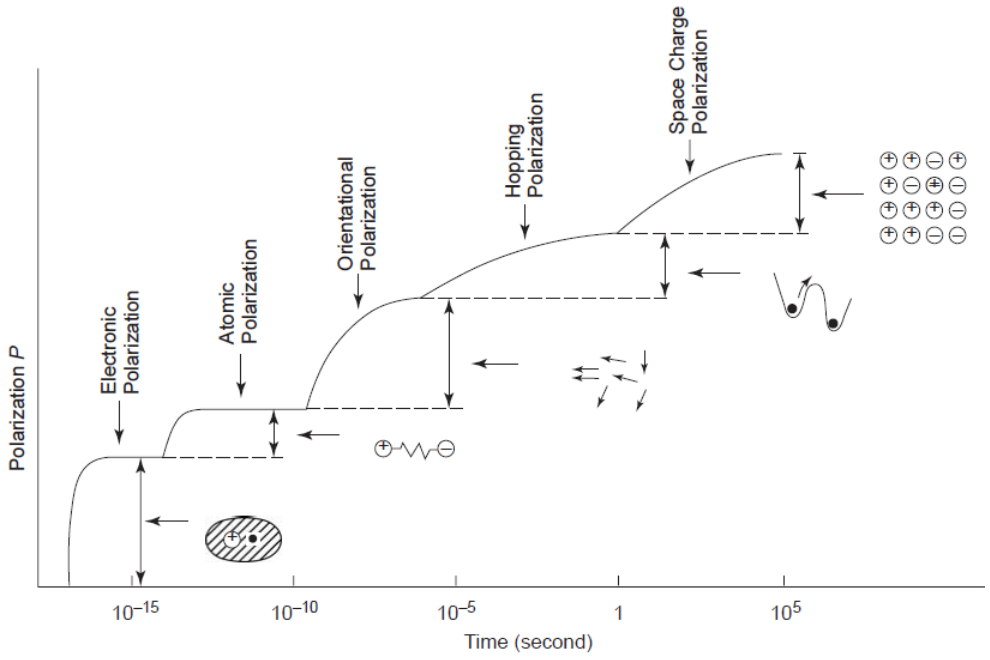



**Figure 1.2** Typical dielectric response to electric field – The variation of different types of polarization with time [19].

properties of SNO are examined using a MOS capacitor structure with a gate insulator of a SNO thin film and the possibility of the memory application of a SNO film is also investigated for the first time.

Since 1960s, memories based on use of ferroelectricity have been studied due to their possibilities as a universal memory [10], [11]. This interest resulted from their small cell sizes with a single element, fast transition time, low power consumption, and nonvolatility [12]. In spite of many attempts, however, the ideal ferroelectric memory using a standard CMOS technology has not been realized. A fundamental issue with the use of ferroelectric materials placed on a semiconductor, or anything non-metallic, is the existence of depolarization field [3], which slowly degrades stored information. When a ferroelectric material is inserted between metal plates, there is no

depolarization field due to the charge compensation by image charges in metal plates. On the other hand, in case of a ferroelectric field effect memory transistor, it is believed that depolarization field always exists due to the finite dielectric constant of a semiconductor [13]. As a solution to this issue, a single crystal and single domain ferroelectric material with "square" P-E hysteresis curve has been studied [12], [20]. The remnant polarization of a film with "square" P-E hysteresis will not be deteriorated by the depolarization field unless it is above the coercive field of the film. This film is, however, too ideal and theoretical to realize. Therefore, ferroelectric memories are expected to be more adequate for dynamic random access memory (DRAM) applications. Indeed, ferroelectric dynamic random access memory (FeDRAM) technology has been proposed as an alternative to the conventional DRAM [13], [14].

In the operation of a FeDRAM, memory window is determined by the remnant polarization ($P_r$), the thickness (t) and the dielectric constant (κ) of a ferroelectric film as the below [21].

$$\Delta V_{th} = \pm P_r t / \kappa \varepsilon_0 \,, \tag{1.2}$$

where the ± sign denotes the direction of the polarization. Hence, to increase the memory window, one employs a ferroelectric material with high remnant polarization and low dielectric constant. Most inorganic ferroelectric materials have high remnant polarizations, but have high dielectric constants. So, ferroelectric polymers have recently been studied as alternatives to perovskite ferroelectric materials because of their low dielectric constants [21].

$VO_2$ has a distorted rutile structure in which a vanadium ion has moved away from the center of an oxide octahedron. The lengths of long and short bonds in $VO_2$ are 2.03, 2.01, 2.05Å, and 1.86, 1.87, 1.76Å, respectively [22]. These off-centered displacements result in a net dipole moment, which suggests that $VO_2$ is likely to be a ferroelectric material. It is known that vanadium pentoxide ($V_2O_5$) is a ferroelectric material with Curie temperature ($T_c$) of 230 ˚C [23]. Meanwhile, $VO_2$ has been studied extensively for its metal-insulator transition and their possible use because of the change in properties arising from changes in conductivity, reflectivity, etc. Ferroelectricity of $VO_2$ has not been studied seriously, although suspected [22], because the metal-insulator phase transition properties are so profound and accessible and different from other materials. In FCC-crystalline phase, GST has a distorted rocksalt-like structure with a lattice parameter of 6.02 Å. In the structure, Ge atoms shift from the ideal rocksalt positions, with Ge-Te bonds in two lengths: 2.80 and 3.13 Å [24], [25]. These off-centered displacements result in a net dipole moment. This suggests that FCC GST is a ferroelectric material. The super-resolution effect in CD/DVD recording media also provides supporting evidence to the presence of ferroelectric transition [26], [27]. Like the ferroelectric polymers, $VO_2$ and GST have a low dielectric constant of around 40 [28], [29], and so are of special interest. In this thesis, the ferroelectricity of $VO_2$ and GST is investigated using a MOSFET structure with a gate insulator of a $VO_2$ or GST thin film and the possibility of the ferroelectric memory application is also discussed.

## *1.3 Organization of Dissertation*

The organization of this dissertation is as follows. Chapter 2 discusses the operation principles of phase transition memory including basic concepts, a simple model, simulation results, and necessary conditions for phase transition materials. In Chapter 3, it describes the material properties of phase transition materials used in the experiments. Chapter 4 depicts the fabrication of bulk-type devices and suspended channel devices with air-gap under the channel. Experiment results of bulk-type devices are discussed in Chapter 5. It includes the results of $VO_2$, GST and SNO devices. Chapter 6 discusses the heat transfer efficiency of each type of transistor and the characterization of GST suspended channel transistors. In Chapter 7, new applications of phase transition materials are presented. A summary of the research and future perspectives for phase transition memory devices are given in Chapter 8.

# Chapter 2

# OPERATION PRINCIPLES OF PHASE TRANSITION MEMORY

This chapter introduces the operation principles of phase transition memory with a gate insulator composed of a phase transition thin film and two silicon dioxides layers. A simple toy model is presented and the results of device simulation and thermal simulation are discussed. The necessary conditions of phase transition materials required for the realization of a phase transition memory and ideal thermal hysteresis property are suggested. Some real phase transition materials are exemplified and their properties are scrutinized. Using a simple thermal conduction model, the switching energy and time of a phase transition memory are estimated.

## *2.1 Basic Concepts and a Simple Model*

The memory cell of a phase transition memory is composed of a single transistor with a similar structure to the cell transistor of a Flash memory as shown in Figure 2.1. In the place of floating gate, a phase transition film is employed as an intermediate gate insulator and sandwiched between two silicon dioxide layers. Therefore, the device has the gate stack of Metal-Insulator-Phase transition material-Insulator-Semiconductor (MIPIS). The phase transition in the material takes place through Joule heating of the device as a result of current flow through the channel.

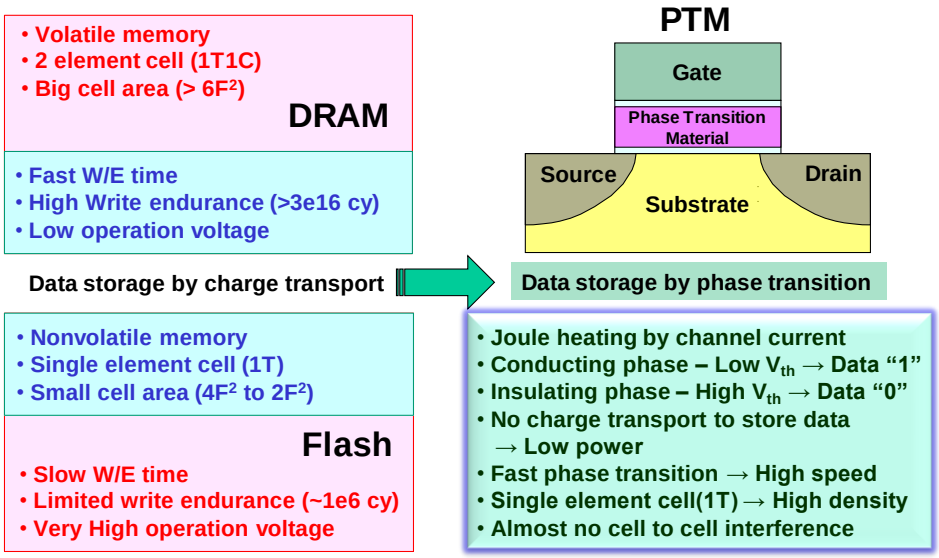



**Figure 2.1** Features and schematic of a phase transition memory transistor.

While the channel current is flowing, the Joule heat occurs and can transfer to the phase transition material through the bottom silicon dioxide. The dissipated thermal energy is utilized to write the data, and erase the data with use of temperature-time profiles that come about from the passage of current with applied waveforms of bias voltages. If the transferred thermal energy is high enough to switch the phase of the material, the transistor properties can be changed due to the variation of equivalent oxide thickness (EOT). This variation results from the change of the dielectric constant induced by the phase transition. In the conducting phase, the phase transition material has a higher dielectric constant and hence the transistor has a higher capacitance resulting in a lower threshold voltage. In the insulating phase, the transistor has a higher threshold voltage by the opposite mechanism: lower dielectric constant and hence lower capacitance. Therefore, the transistor can store one binary bit (0 or 1) in accordance with the phase of the material. That is, the phase transition

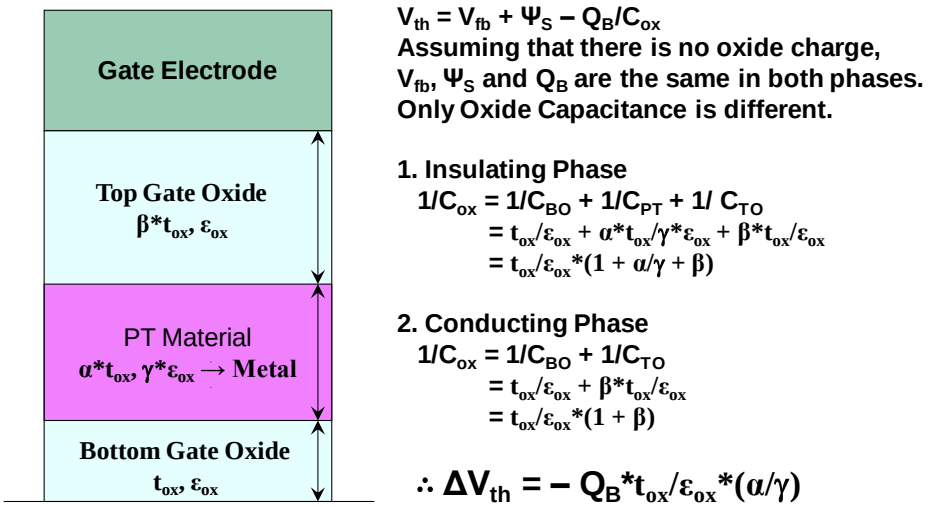



**Figure 2.2** A simple model for a phase transition memory.

material plays a role of a memory node. The proposed device is a new form of memory based on phase transition in a single element. The new approach takes advantage of the fact that information can be stored by the thermally-induced phase transition of the material without resorting to charge storage. That is, there is no need for charge transport into a memory node to store information. An interest in a universal memory with a small cell size in a single element, fast transition time, low power consumption and nonvolatility has driven the invention of many structures of novel memory devices and the new application of various materials. This phase transition memory is invented as part of the efforts.

Figure 2.2 shows the simple model for a phase transition memory. The threshold voltage ($V_{th}$) of a MOSFET is defined by Equation 2.1.

$$V_{th} = V_{fb} + \Psi_S - \frac{Q_B}{C_{ox}}, \tag{2.1}$$

where $V_{fb}$ is the flat band voltage, $\Psi_S$ is the surface potential that is equal to $2\Psi_B$, $Q_B$ is the depletion region charge in the substrate, and $C_{ox}$ is the capacitance of the gate. Suppose that there is no oxide charge and $V_{fb}$, $\Psi_S$ and $Q_B$ are the same in both phases. That is, only the dielectric constant and conductivity of the phase transition material is assumed to be different between two phases and in the metallic state, the permittivity to be infinite. From these assumptions, the threshold voltage difference between two phases is determined by the variation of gate capacitance as shown in Figure 2.2.

$$\Delta V_{th} = -Q_B \times t_{ox} \times \varepsilon_{ox} \times \left(\frac{\alpha}{\gamma}\right), \tag{2.2}$$

where $t_{ox}$ is the thickness of bottom silicon dioxide, $\varepsilon_{ox}$ is the permittivity of silicon dioxide, $\alpha$ is the thickness ratio of phase transition film to bottom oxide, and $\gamma$ is the permittivity ratio of phase transition film to bottom oxide. According to Equation 2.2, $\Delta V_{th}$ is determined by the thickness and dielectric constant of a phase transition material. In detail, $\Delta V_{th}$ is proportional to the thickness and inversely proportional to the dielectric constant in the insulating phase.

## *2.2 Device and Thermal Simulation*

Device and thermal simulations have been performed to confirm the operation of a phase transition memory using ATHENA and ATLAS from SILVACO International. ATHENA simulator has been used to optimize semiconductor processes and ATLAS simulator has been used to simulate the electrical and thermal behaviors of semiconductor devices. Figure 2.3 (a) shows the schematic cross-section and net doping profile of a transistor employed for the device simulation on the p-type

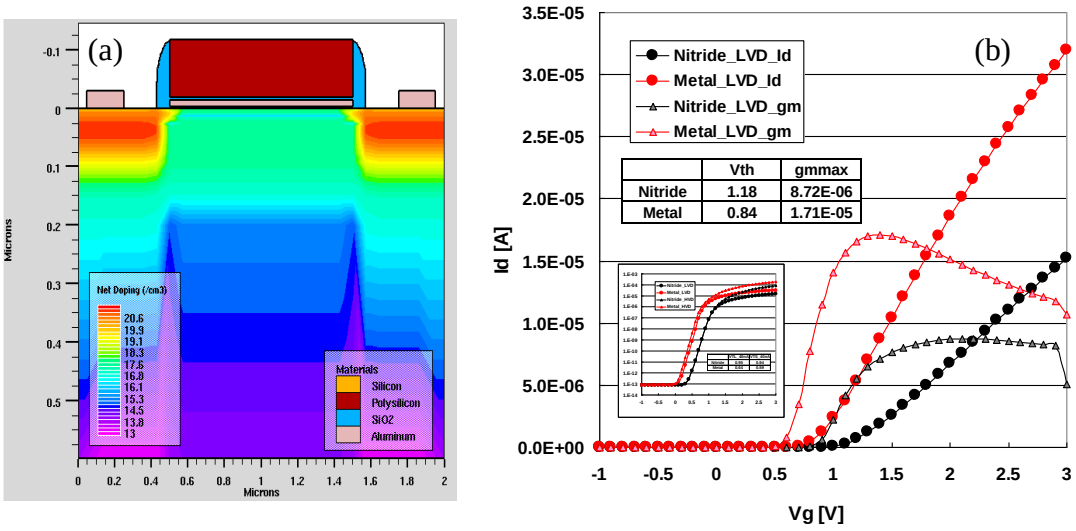
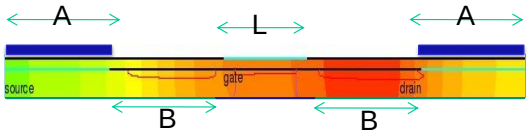



**Figure 2.3** Device simulation results: (a) schematic cross-section and net doping profile of a transistor and (b) difference of threshold voltage between two phases.

substrate with 100 orientation and boron doping density of 1 x $10^{14}$ $cm^{-3}$. The gate length is 1 μm of physical length and the gate dielectric layer consists of bottom silicon oxide (2 nm), phase transition film (6 nm), and top silicon dioxide (4 nm). An n+ phosphorous polysilicon layer with the thickness of 100 nm is deposited. To simulate the phase transition effect, silicon nitride is used in the insulating phase as a phase transition film and aluminum is used in the conducting phase. To adjust the threshold voltage, the channel implantation process is executed using B and $BF_2$. The boron concentration at silicon surface is 1 x $10^{18}$ $cm^{-3}$ after channel implantation process and it is diffused and the doing density is lowered to 5 x $10^{17}$ $cm^{-3}$ after anneal treatment in nitrogen environment for 60 minutes at 900 ℃. Figure 2.3 (b) shows the difference of threshold voltage between two phases, which is ~0.34 V. This is in good agreement of the calculation (~0.35 V) using the simple model presented in the




| L (Leff) [nm] | A/B [nm] | Lattice Temp. [K] Gate oxide / Highest (VG=VD=1V) | Lattice Temp. [K] Gate oxide / Highest (VG=VD=4V) | Current [uA/um] Vg=Vd=1V |
|---|---|---|---|---|
| 100 (90) | 250/250 | 310 | 526/543 | 205 |
| | 50/50 | | 980/1075 | 346 |
| 40 (29) | 250/250 | 310/430 | 588/593 | 282 |
| | 50/50 | 458/465 | 1190/1267 | 561 |
| | 250/50 | 428/435 | 1074/1095 | 639 |

**Figure 2.4** Thermal simulation results performed by non-isothermal device simulator of Giga.

previous section.

To perform a thermal simulation, Giga, a component of the ATLAS device simulation framework, has been used. Giga is combined with S-Pisces and Blaze device simulators. The heat equation of mathematical model for heat transfer by conduction is as follows [30].

$$\rho C \frac{\partial T}{\partial t} - \nabla \cdot (k \nabla T) = Q \,, \tag{2.3}$$

where $\rho$ is the density, $T$ is the temperature, $C$ is the heat capacity, $k$ is the thermal conductivity, $t$ is the time and $Q$ is the heat flux. The heat generated by Joule heating Q is given by Equation 2.4.

$$Q = \frac{1}{\sigma} |J|^2 = \sigma |\nabla V|^2 \,, \tag{2.4}$$

where $\sigma$ is the electric conductivity, $J$ is the electric current density and $V$ is the electric potential. Figure 2.4 shows the results of thermal simulation performed by

Giga. The lattice heating model assuming non-isothermal conductivity is used. That is to say, the electron and hole current densities are modified to account for spatially varying lattice temperatures. A transistor on the SOI substrate is simulated and the thickness of top silicon is 5 nm. The thickness of gate oxide is 2 nm and the doping densities of channel and S/D are $1.75 \times 10^{17}$ and $1 \times 10^{20}$ $cm^{-3}$, respectively. When the gate length is 40 nm, the threshold voltage is ~0.39 V, which is similar to that of an IBM 30 nm transistor with a similar gate structure. As shown in the figure, the temperature of gate oxide is over 500 K at every split corner when $V_G$ and $V_D$ are 4 V. This implies that the thermal energy transferred to a phase transition material is high enough to switch the phase of the material with phase transition temperature under 500 K. The space between gate and S/D contacts is a dominant factor for the temperature distribution. In case of 50 nm space, the temperature of gate oxide reaches around 1000 K irrespective of gate length. As a result, it is likely that Joule heating induced by the channel current results in the phase transition of the material inserted in between silicon dioxide layers.

## *2.3 Necessary Conditions of Phase Transition Materials*

To realize a phase transition memory, there are several necessary conditions for phase transition materials. Firstly, for a room temperature operation, a phase transition material needs to have a thermal hysteresis as shown in Figure 2.5. The heating-up transition temperature is above room temperature and the cooling-down transition temperature is below room temperature. For the erase operation, the cooling-down transition temperature should be tunable and increased above room temperature.

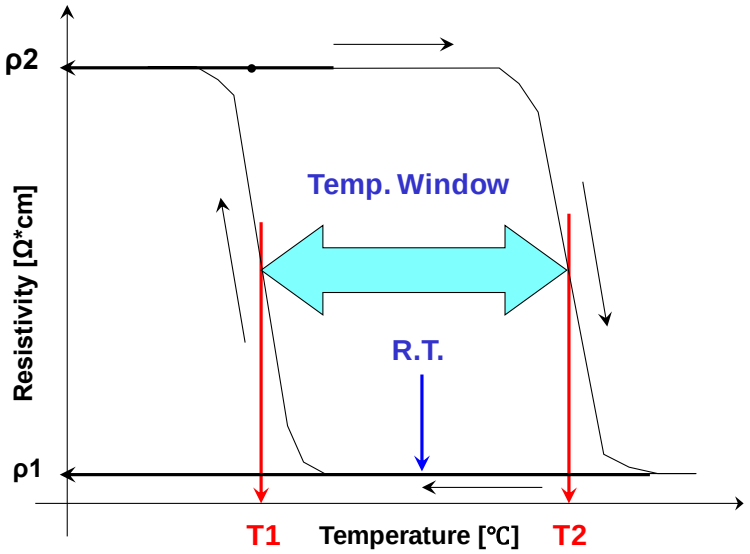



**Figure 2.5** Ideal thermal hysteresis curve.

The possibility that the transition temperature of $VO_2$ can be increased by an electrical field has been presented by Chudnovskiy et al. [31]. They argued that the effect is stronger for thinner films, since the capacitance increases and the transition entropy decreases. After the memory transistor turns on, the write operation is established by Joule heat in the channel. When thermal energy transferred to the phase transition material is enough for the phase transition, the material becomes metallic and keeps its metallic phase after the transistor turns off because the cooling-down transition temperature is below room temperature. For the erase operation, the electric field applies to the phase transition material and then the transition temperature becomes higher than room temperature. Hence, the material returns to the insulating phase. To store information stably, wide temperature hysteresis window is needed.

Secondly, a phase transition material needs to have a fast transition time. Phase transition time ($t_{tr}$) is a very critical factor on data writing process. Bit Switching is

the result of the phase transition induced by the Joule heating in the channel of a memory transistor. Therefore, the switching time is determined by Equation 2.5.

$$\alpha I_{dsat} R_{ch} t_{tr} = m_{ox} C_{ox} \Delta T + L_{PT} V_{PT} \,, \tag{2.5}$$

where $\alpha$ is the heat transfer efficiency, $I_{dsat}$ is the saturation drain current, $R_{ch}$ is the channel resistance, $m_{ox}$ is the mass of silicon dioxide, $C_{ox}$ is the heat capacity of silicon dioxide, $\Delta T$ is the temperature difference between room temperature and phase transition temperature, $L_{PT}$ is the latent heat of a phase transition material and $V_{PT}$ is the volume of a phase transition material. In this equation, left is a formula of joule heating energy generated by channel current and the first term on the right represents the oxide-heating energy and the second is the latent heat of a phase transition material. Heat transfer efficiency ($\alpha$) is defined by

$$\alpha = \frac{H_{up}}{(H_{up}+H_{down})} = \frac{R_{down}}{(R_{up}+R_{down})} \,. \tag{2.6}$$

In this equation, $H_{up}$ and $H_{down}$ mean heat conductions delivered from the channel upwardly and downwardly, respectively. $R_{up}$ and $R_{down}$ mean heat resistances of corresponding heat conductions. The heat transfer efficiency is around a few percent for a bulk silicon device and around 15 percent for a SOI device. More details about heat transfer efficiency will be discussed in Chapter 6.

Lastly, a phase transition material needs to have a wide memory window that is determined by the threshold voltage difference between an insulating phase and a conducting phase. According to Equation 2.2, $\Delta V_{th}$ is correlated with the thickness and

**Table 2.1** Examples of phase transition materials and their properties.

| | T1 | T2 (ΔT) | ρ1 | ρ2 (Ratio) | ε | L | Transition Factors |
|---|---|---|---|---|---|---|---|
| | [℃] | | [Ω*cm] | | | [J/g] | |
| $VO_2$ | 0 ~ 60 | 20 ~ 70 (10 ~ 20) | 1e-2 ~ 1e-4 | 0.1 ~ 10 (100 ~ 1000) | 36 → 1e4 | 51.46 | Heat E-field |
| GST | - | 150 @ACT 270 @CCT | 25 | 0.025 (1000) | 16 → 38 | 16.2 | Heat |
| Doped IGT | - | 280 ~ 300 | 1000 ~ 1e4 | 1 (Nor.) | | | Heat |
| TMO (NiO) | - | > 300 | 100 ~ 1000 | 1 (Nor.) | | | E-field Heat |
| $CrO_2$ | - | -60 | | | | | Heat H-field |
| $Nb_2O_5$ | 350 | 530 | | | | | Heat H-field |

dielectric constant of a phase transition material. For the large memory window, the thickness of the phase transition film should be increased and the dielectric constant of the phase transition film should be decreased. However, these changes can deteriorate the switching speed of a phase transition memory. According to Equation 2.5, the switching time is correlated with the drain saturation current and the volume of a phase transition material. The increase of the thickness of the phase transition film causes the increases of its volume and the decrease of the drain current resulting in the increase of the switching time. Similarly, the decrease of the dielectric constant causes the drain current decreases resulting in the increase of the switching time increases. As a result, the optimization of these factors might be a challenge for memory applications.

Table 2.1 shows several materials whose phases are changed by heat, electric field or magnetic field. Among them, GST is the most prevalent material used in PRAM, CD and DVD. Its phase can be reversibly switched from the amorphous to the poly-crystalline by Joule heating. GST has two crystalline phases. One is the metastable FCC phase; the other is the stable HCP phase [32], [33]. So, phase transition happens twice. At around 150 ℃, the phase changes from amorphous to FCC crystalline, and at around 270 ℃, it changes from FCC to HCP crystalline. Another famous phase transition material is $VO_2$ that have a large permittivity change occurring together with conductivity change in a thermal and field-activated process. $VO_2$ becomes tetragonal from monoclinic above the transition temperature [34] and is in a metallic state. Resistivity changes of up to 3-5 orders have been observed [35]–[37]. Its transition temperature is near room temperature, around 68 ℃ and thus this thin film has been applied in various electro-optical devices including in temperature controlled reflectors [35], [38]. However, the properties of $VO_2$ thin films are very unstable and irreproducible due to the bad surface morphology and domain structure produced on passing through the phase transition. So, recently, the device application of single domain $VO_2$ nanowires has received much attention [39]–[42].

Using Equation 2.5 and Table 2.1, oxide heating energies, latent heats, Joule heats and switching times of $VO_2$ and GST are estimated as shown Figure 2.6. The heat transfer efficiency is assumed to be 0.5. The thicknesses of bottom gate oxide and top gate oxide are fixed to 10 and 20 nm, respectively. $\Delta T$'s of $VO_2$ and GST are set to 50 and 130 ℃, respectively. In Figure 2.6 (a), oxide heating energy and latent heat is proportional to the square of effective gate length, because the mass of silicon dioxide

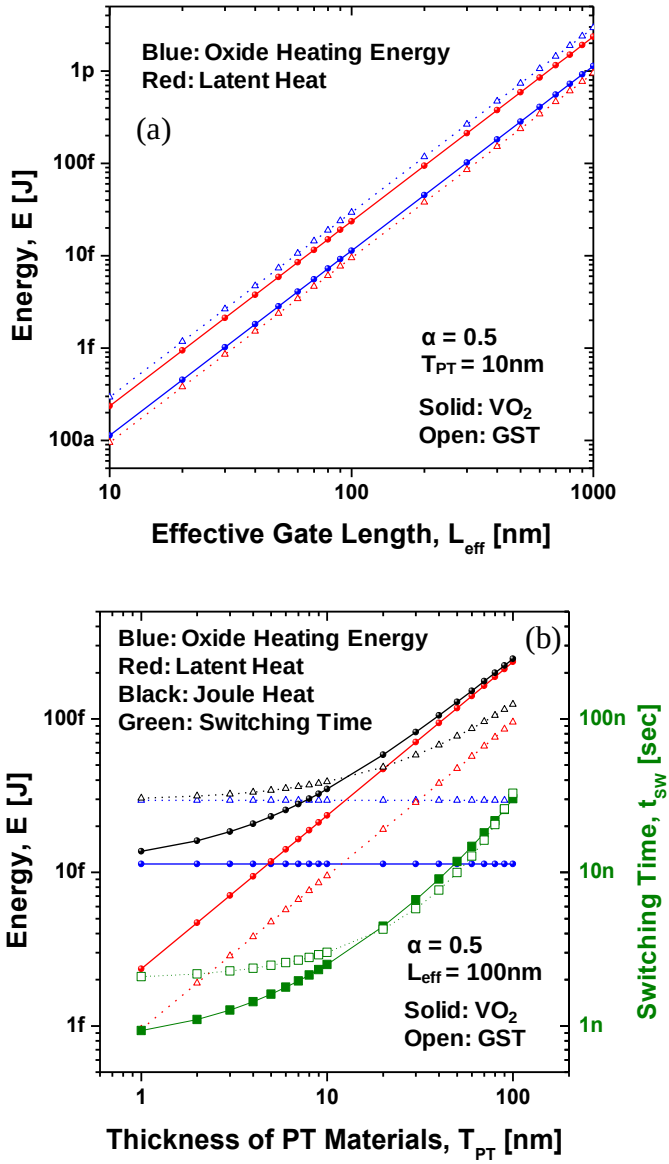



**Figure 2.6** Correlation of energy and switching time (a) with effective gate length and (b) the thickness of a phase transition material.

and the volumes of phase transition materials are quadratic with effective gate length. In view of oxide heating, GST needs more energy compared to $VO_2$. On the other hand, GST has smaller latent heat than $VO_2$. As shown in Figure 2.6 (b), oxide heating energy is independent of the thickness of a phase transition film and latent heat is proportional to the thickness of a phase transition film. Thus, the oxide heating energy

of $VO_2$ is dominant under the thickness of 7 nm and the oxide heating energy of GST is dominant under the thickness of 30 nm. Under the thickness of 10nm, GST needs more Joule heat than $VO_2$. The switching speed of $VO_2$ is faster than that of GST overall except between 20 and 80 nm. In case of 100 nm gate length device with 10 nm of a phase transition film, the switching energy and time are ~40 fJ and ~4 ns, respectively. Considering that the switching energy of a conventional phase change memory is over 100 fJ and the switching time of a conventional DRAM is around 10 ns, the proposed phase transition memory may be able to be a promising candidate for a universal memory.

## *2.4 Summary*

A new phase transition memory with a gate insulator consisting of a phase transition film and two silicon dioxide layers has been proposed. Its operation principles have been discussed along with a simple model and the simulation results. Through the thermal simulation, it has been confirmed that Joule heating induced by the channel current is high enough to cause the phase transition of the material on top of the bottom oxide layer. In terms of thermal hysteresis window, switching time and memory window, necessary conditions of phase transition materials required to make a phase transition memory possible have been reviewed. Among the materials whose phases are changed by heat, electric field or magnetic field, the properties of $VO_2$ and GST have been examined. Using a simple thermal conduction model, the switching energies and times of $VO_2$ and GST have been extracted and analyzed. The Joule heat

of ~40 fJ and the switching time of ~4 ns are expected in the proposed phase transition memory, which are superior or compatible to those of other memories.

# Chapter 3

# PHASE TRANSITION MATERIALS

This chapter focuses on the phase transition materials used in the experiments; Vanadium Dioxide ($VO_2$), Germanium Antimony telluride ($Ge_2Sb_2Te_5$, GST) and Samarium Nickelate ($SmNiO_3$, SNO) are employed as intermediate gate insulators. Their transition mechanisms and physical properties are discussed and the composition stoichiometric and surface morphologic analyses are performed. The temperature dependences of their resistances are characterized.

## *3.1 Vanadium Dioxide, $VO_2$*

### 3.1.1 Transition mechanism and physical properties of $VO_2$

$VO_2$ is a representative correlated electron oxide material with phase transition close to room temperature. The phase transition takes place rapidly – about the order of picosecond [31]. A large conductivity change occurs together with a permittivity change in a thermal or field-activated process [43]–[48]. Typical transition temperature is around 68 ℃ and resistivity changes of up to 3-5 orders have been observed. The transition temperature and hysteresis window can be tuned by W-doping, pressure and stress [49]–[52]. The phase transition results from the change of crystal structure as shown in Figure 3.1. Above the transition temperature, $VO_2$ is a metal and isomorphic to $TiO_2$ with a tetragonal rutile structure [53], [54]. The vanadium atoms are surrounded by an octahedron of 6 oxygen atoms. The oxygen

(a) Metallic Phase (T > 68 ℃)
Tetragonal rutile structure

(b) Insulating Phase (T < 68 ℃)
Monoclinic structure

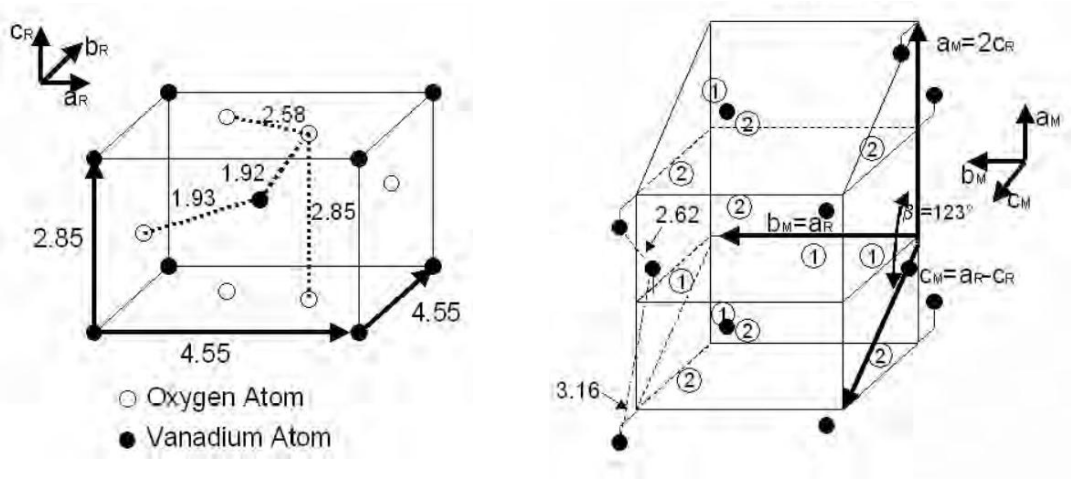



**Figure 3.1** Crystal structures of $VO_2$: (a) Tetragonal rutile structure in the metallic phase and (b) monoclinic structure in the insulating phase and its relationship to the rutile structure. Circled 1 and 2 depict the positions of the oxygen atoms before and after the phase transition [54].

atoms located in the surfaces vertical to the $c_R$ axis are shared by two adjacent octahedra and hence the shortest V-V distance is along the $c_R$ axis. As the temperature decreases, the crystal structure of $VO_2$ distorts and becomes monoclinic, isomorphic to $MoO_2$. Below the transition temperature, $VO_2$ is an insulator or semiconductor with a band gap of ~0.7 eV as shown in Figure 3.2. The phase transition causes the change of its electronic structure, which can be detected by photoemission spectroscopy [54]. In a simple orbital picture, these structural changes influence the V 3d $t_{2g}$-derived states [55]–[57], which fall into the $d_{\|}$ orbital and the $\pi$ orbital [53]. While the $d_{\|}$ bands split into occupied bonding and empty anti-bonding states, the $\pi$ states shift up in energy leading to their depopulation [56], [57]. As a result, a band gap is formed at the Fermi level between the bonding $d_{\|}$ and $\pi$ bands.

(a) Metallic Phase (T > 68 ℃)
Tetragonal rutile structure

(b) Insulating Phase (T < 68 ℃)
Monoclinic structure

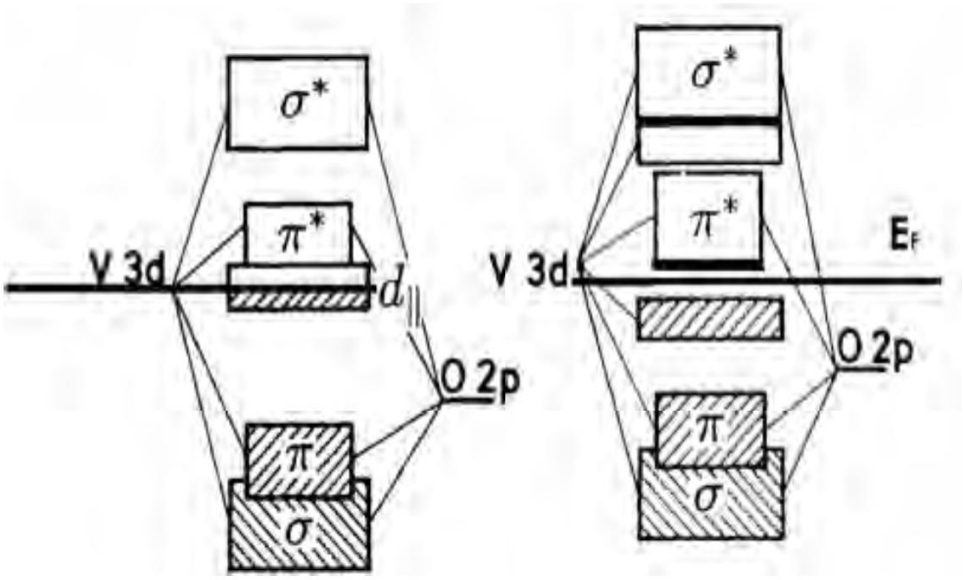



**Figure 3.2** Band Diagrams of $VO_2$: (a) Metallic phase and (b) insulating phase with a band gap of ~0.7 eV [54].

Since the metal-insulator phase transition phenomenon of $VO_2$ was discovered by Morin [44], several models have been proposed to describe it [58], [59]. Besides Peierls model that describes the phase transition by thermal excitation [60], [61], Mott-Hubbard model argues that the electron concentration, instead of temperature, is the controlling parameter for the MIT in $VO_2$ [45], [62]. Moreover, Cavalleri et al. showed an optically driven MIT phenomenon using femtosecond x-ray and visible pulses to probe structural and electronic dynamics [63]. Lim et al. reported that the geometric structural change does not happen during electronic excitation [64]. With the increase of the applied electric field, valence electrons tunnel through the potential barrier into the conduction band. Once the injected electron density reaches the critical

value, the phase transition takes place and a metallic state is formed. Chudnovskii et al. estimated that the threshold field for the transition is about 100 ~ 500 kV/cm [65]. Therefore, the metal-insulator phase transition of $VO_2$ can be initiated not only by a thermal excitation, but also by photonic excitation or a high electric field.

### 3.1.2 Composition and surface analysis

Vanadium has numerous oxidation states (+2, +3, +4 and +5) and thus there are several vanadium oxides [66]: vanadium monoxide (VO), vanadium trioxide ($V_2O_3$), vanadium dioxide ($VO_2$), and vanadium pentoxide ($V_2O_5$). In addition to these principle oxides, various other distinct phases exists: Magneli phases ($V_nO_{2n-1}$) between $V_2O_3$ and $VO_2$ such as $V_4O_7$, $V_5O_9$, $V_6O_{11}$, $V_7O_{13}$ and $V_8O_{15}$, and phases ($V_nO2_{n+1}$) between $VO_2$ and $V_2O_5$ such as $V_3O_7$, $V_4O_9$ and $V_6O_{13}$. Moreover, there exist many non-stoichiometric vanadium-oxygen phases. Therefore, it is very difficult to grow a pure vanadium dioxide film and coexistent oxide phases can degrade the phase transition property of the $VO_2$ film. In the experiment, vanadium dioxide thin films are deposited with a DC reactive sputtering process in Ar (91.2%) + $O_2$ (8.8%) environment at 10 mTorr from a V target. The base pressure in the sputtering chamber is $2 \times 10^{-8}$ Torr and the substrate temperature is kept at 550 ℃ during the deposition. After the deposition, the $VO_2$ samples are transferred to the load lock and cool down rapidly to minimize post-deposition annealing, which is believed to improve the phase transition property [67].

To confirm the composition stoichiometry of the deposited $VO_2$, X-ray photoelectron spectroscopy (XPS) analysis is performed. The metal-insulator phase

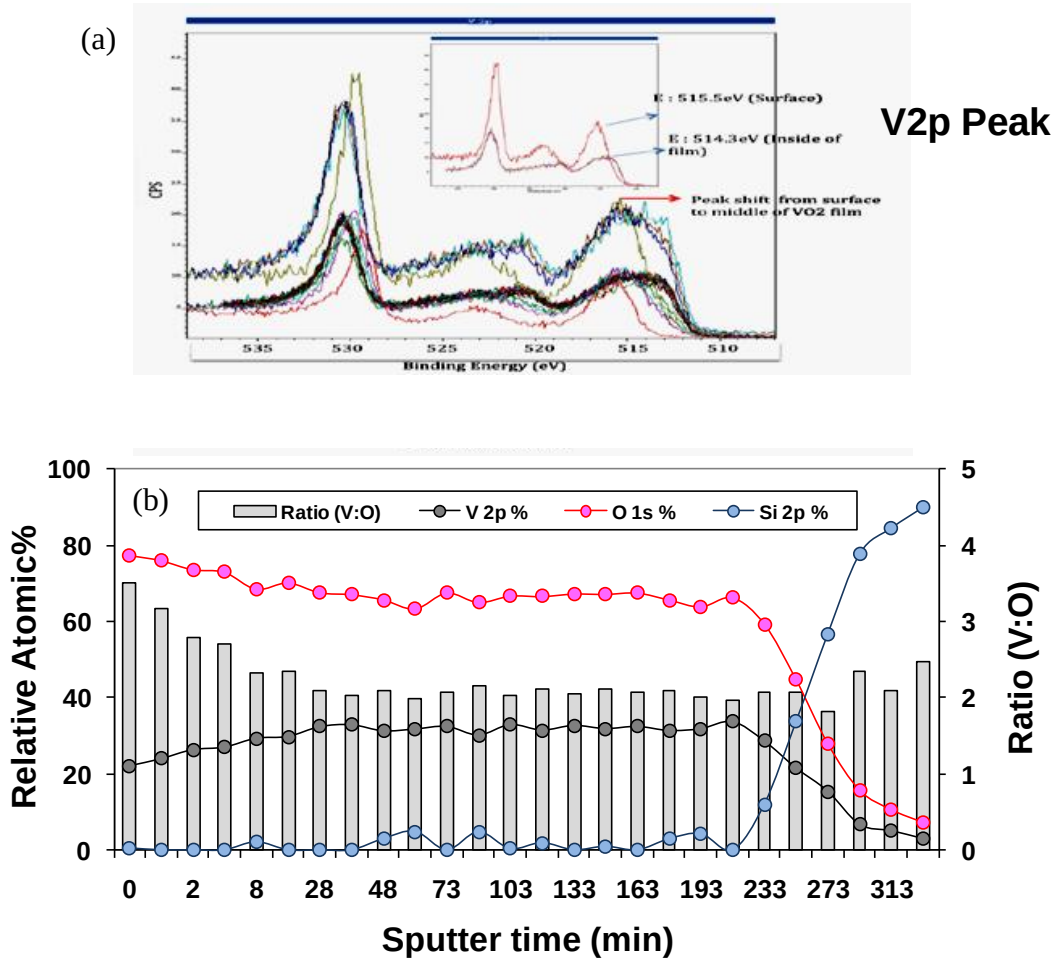



**Figure 3.3** XPS analysis for (a) V(2p) signal and (b) relative atomic ratio of V(2p) to O(1s). Binding energy of V(2p) peaks vary from 515.5 eV (film surface) to 514.3 eV (inside of the film) and the ratio of V(2p) and O(1s) is 1:2.1 and 1:3.3 in the middle and surface of the film, respectively.

transition of the $VO_2$ film is also directly measured through conductivity measurement. Super-saturation multi-phase effects here are reflected in the thermal hysteresis observed. Figure 3.3 (a) shows that V(2p) peaks at binding energy vary from 515.5 eV (film surface) to 514.3 eV (inside of the film). Normally, V(2p) peak is around 515 eV. The atomic composition ratio of V(2p) to O(1s) is shown in Figure 3.3 (b). The ratio is around 1 to 2.1 in the middle of the film and 1 to 3.3 on the surface. This implies that

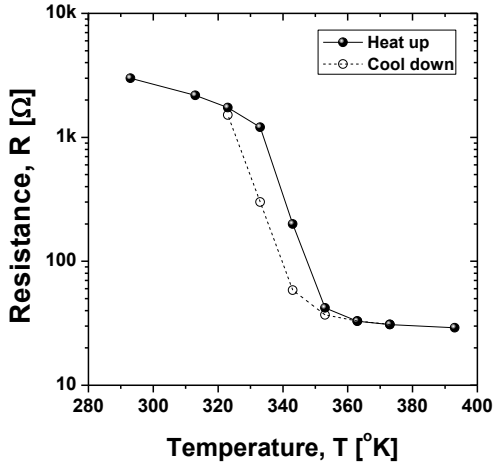



**Figure 3.4** Thermal hysteresis of the resistance of $VO_2$ film. The phase transition of $VO_2$ occurs at around 70 ˚C, which is the typical transition temperature of $VO_2$.

the vanadium oxide film in our experiments is composed of the family of various vanadium oxides depending on the sputtering temperature and oxygen gas flow rate.

Although the atomic composition ratio acquired from the XPS analysis is not exactly 2, the film has a typical thermal hysteresis behavior of the resistance of $VO_2$ as shown in Figure 3.4. The phase transition occurs at around 70 ℃, which is the typical

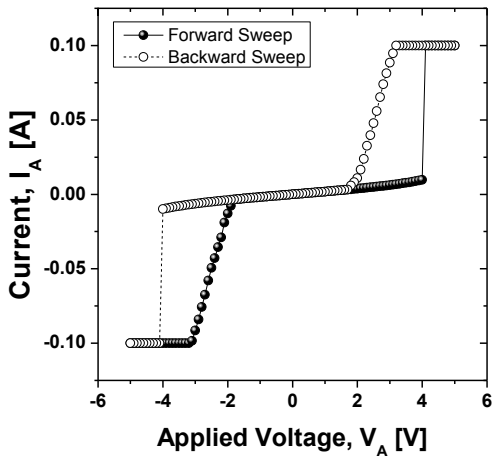



**Figure 3.5** Mott transition property of $VO_2$ film. Phase transition of $VO_2$ occurs at high current injection state even at room temperature.

phase transition temperature of $VO_2$. In addition, the current induced phase transition effect commonly measured in stacked structures (here laterally) is also observed as shown in Figure 3.5. This is the Mott-Hubbard transition property of $VO_2$ [11]. The phase transition of $VO_2$ happens at the high current injection state even at room temperature. From the above results, it is obvious that $VO_2$ oxide phase dominates the other oxidation states in the film used in the experiments.

The surface morphology and roughness of a $VO_2$ film are examined using a Scanning Electron Microscope (SEM) and an Atomic Force Microscope (AFM) as shown in Figure 3.6. Grain size of $VO_2$ is about 100 ~ 500 nm. On a 5 μm x 5 μm

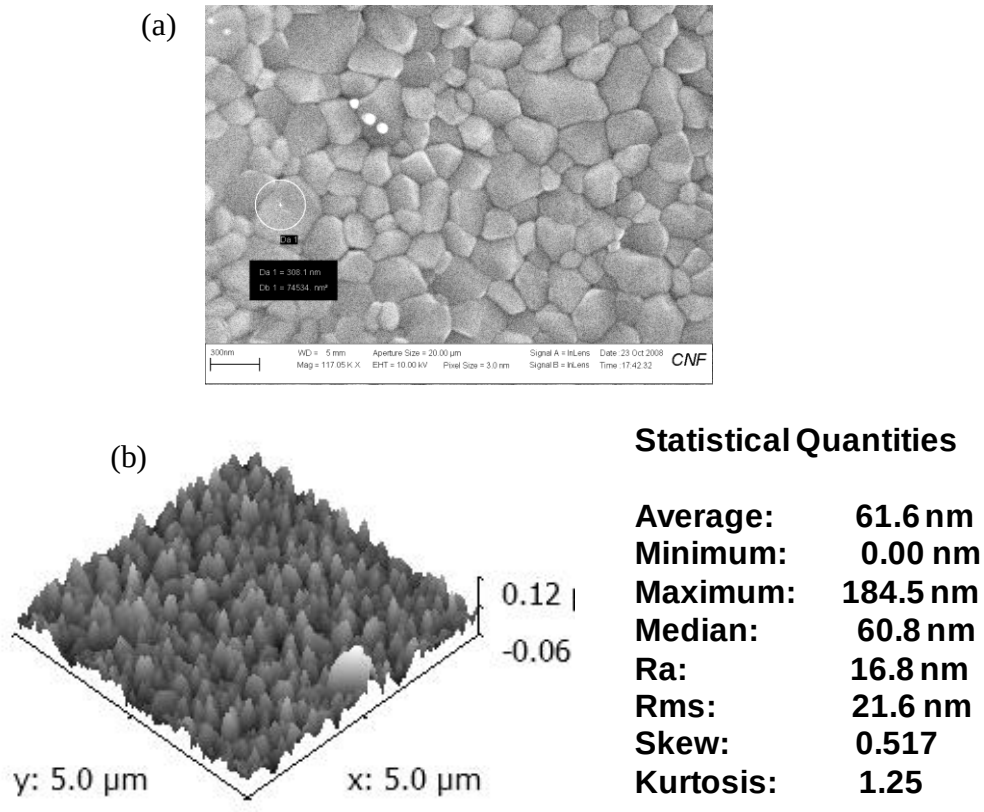



**Figure 3.6** Surface morphology and roughness of a $VO_2$ film examined by (a) SEM and (b) AFM.

AFM scanning area, the average roughness ($R_a$) and root mean square (RMS) roughness are 16.8 and 21.6 nm, respectively, which are 8.4 and 10.8 % of the thickness of the $VO_2$ film. This roughness value is much bigger than the roughness (~2 nm) of an amorphous silicon film deposited by plasma enhanced chemical vapor deposition (PECVD) as a floating gate layer [68]. In view of electronic device application of $VO_2$, multi-phase effects and the bad surface morphology should be improved to get a stable device operation. The $VO_2$ film has hysteresis characteristics with ~30 ℃ of temperature window and its phase transition occurs ~70 ℃ with the resistance change of $10^2$ Ω, which is not comparable with well qualified $VO_2$ films. This is likely due to the presence of uneven surface and non-stoichiometric composition of sputtered $VO_2$ films.

### 3.1.3 Ferroelectricity of $VO_2$

Orgel argued that the ferroelectricity of transition metal oxides can be induced by the off-centered displacement of metal ions at the center of an oxide octahedron [22]. $VO_2$ has a distorted rutile structure in which a vanadium ion has moved away from the center of an oxide octahedron. The lengths of long and short bonds in $VO_2$

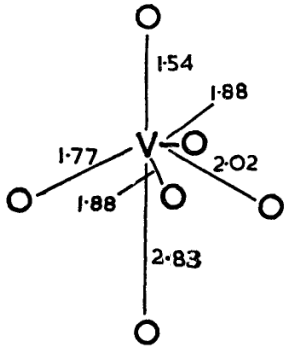



**Figure 3.7** The oxide octahedron surrounding $V^{5+}$ cation of $V_2O_5$ [23].

are 2.03, 2.01, 2.05 Å, and 1.86, 1.87, 1.76 Å, respectively. These off-centered displacements result in a net dipole moment, which suggests that $VO_2$ is likely to be a ferroelectric material. Among other vanadium oxides, $V_2O_5$ is the most stable and common oxide compound. The structure of $V_2O_5$ suggested by Byström et al. is illustrated in Figure 3.7 [69]. The $V^{5+}$ cation is distorted from regular octahedral and the sixth oxide is at the great distance of 2.83 Å from the $V^{5+}$ cation. The distortion induces a net dipole moment and thus $V_2O_5$ can be ferroelectric. Ismailzade et al. proved that $V_2O_5$ is a ferroelectric n-type semiconductor with Curie temperature ($T_c$) of 230 ℃ and band gap of 1 eV [23]. As discussed in Chapter 1, to increase the memory window of a ferroelectric memory, low dielectric constant is needed. $VO_2$ has a low dielectric constant of around 40 compared to perovskite ferroelectric materials, and so is of special interest.

## *3.2 Germanium Antimony Telluride, $Ge_2Sb_2Te_5$*

### 3.2.1 Transition mechanism and ferroelectric properties of GST

GST is ubiquitous in rewritable optical storage media and being employed in nonvolatile phase change memories. In the latter, fast transition times, large sensing margins, good scalability, and CMOS compatible processing superior to other phase change materials have led to widespread interest [70]–[72]. The phase transition employed in these structures is structural: between amorphous and crystalline phases leading to conductivity change and achieved by the widths of current pulses that create heat through ohmic dissipation. GST undergoes two structural phase transitions: amorphous-to-FCC lattice at ~150 ℃ and FCC-to-HCP lattice at ~250 ℃. The phase

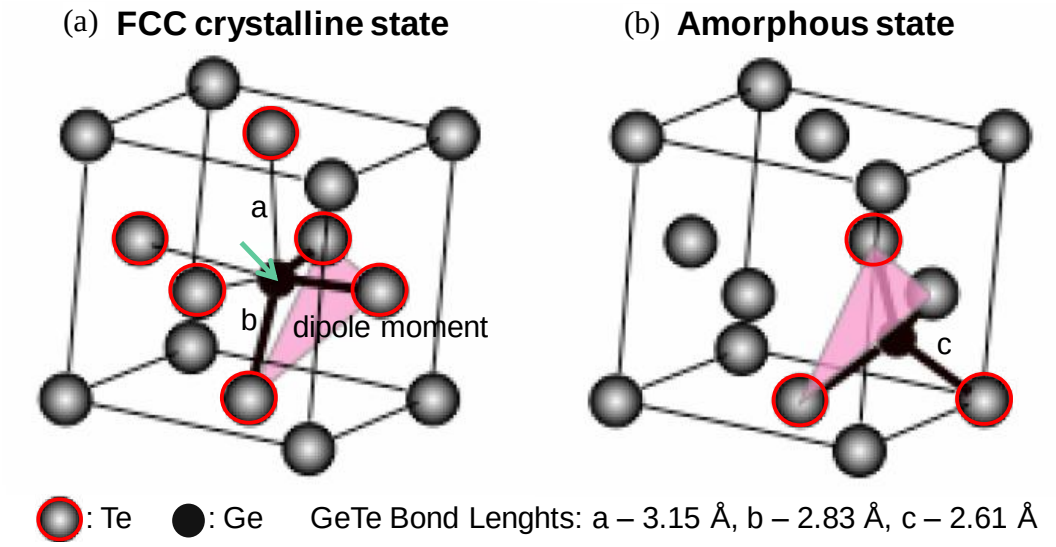



**Figure 3.8** Local structures of GST in (a) the FCC crystalline and (b) the amorphous states [71].

transition mechanisms of GST have not been fully understood yet and so the analysis of experiment results often requires wide-ranging assumptions about the atomic arrangements. The meta-stable nature of amorphous GST has also been a burden for experimental studies of this material. Therefore, a number of studies focusing on a restricted ranges of structures using unit cells (typically ~ 60 atoms) have been performed on GST materials in recent years, and they have provided important clues to the phase transition mechanism [73], [74]. However, they have not explained the details of the mechanism. Kolobov et al. suggested the localized structural transformation model of GST as illustrated in Figure 3.8 [70], [71]. In FCC crystalline phase, a Ge atom is located at the center of the octahedron formed by Te atoms. By a thermal excitation, the Ge atom shifts from the octahedral to tetrahedral symmetry position. The thicker lines stand for stronger covalent bonds in the figure. An intense

thermal stimulation induces the breaking of the weaker bonds and the Ge atom flips into the tetrahedral position.

This local structure model provides a clear explanation for the unusual band gap change and ferroelectricity of GST. Typically, amorphization results in bond-weakening and the generation of tail states leading to the decrease of the band gap [75]. Therefore, absorption and reflectance coefficients in the amorphous state increase due to the decrease of the band gap. However, GST in the crystalline state has a smaller band gap and higher reflectance than in the amorphous state. Indeed, the crystalline GST has shorter and longer Ge–Te bonds as shown in Figure 3.8. The longer bond has weaker covalent bonding energy and thus a smaller energy splitting between the bonding and antibonding states, which determines the width of the band gap in the crystal [71]. On the other hand, the amorphous GST has no weaker bonds and thus a larger band gap. In FCC phase, GST has a distorted rocksalt-like structure with a lattice parameter of 6.02 Å. As shown in Figure 3.8 (a), Ge atoms shift from the ideal rocksalt positions, with Ge-Te bonds in two lengths: 2.83 Å and 3.15 Å. These off-centered displacements result in a net dipole moment. This suggests that FCC GST is a ferroelectric material. The super-resolution effect in CD/DVD recording media, a non-diffraction limited recording resolution improvement arising from high refractive index changes, also provides supporting evidence to the presence of ferroelectric transition in the vicinity of Curie temperature ($T_c$) [26], [27]. In addition, such chalcogenide materials as GaGeTe, SnTe and GeTe, which have narrow bandgaps and similar resistivities to that of FCC GST, have been known as semiconducting ferroelectric materials [76]-[78]. Figure 3.9 (a) shows the resistance and dielectric

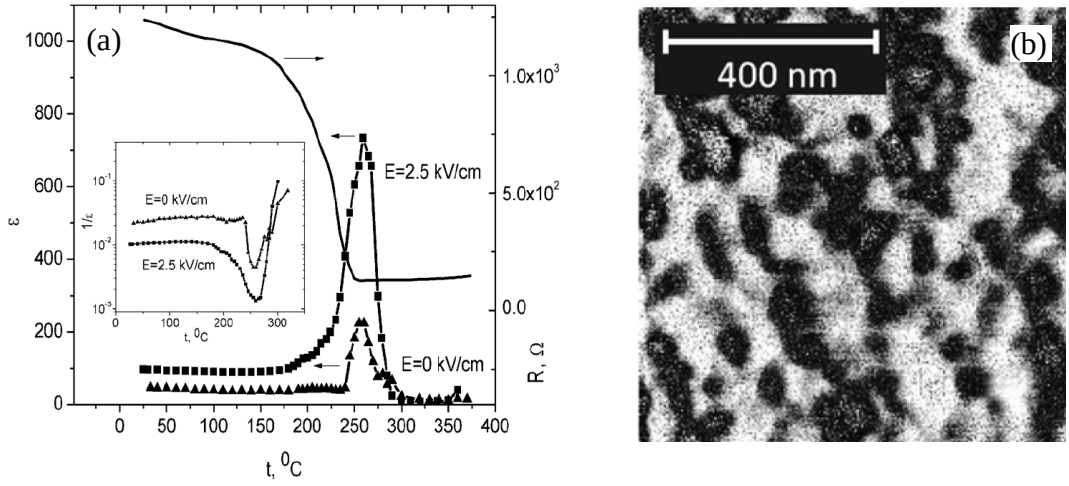



**Figure 3.9** Ferroelectricity of FCC GST films. (a) Resistance (continuous line) and dielectric constant (points) as a function of temperature; inset shows the reciprocal dielectric constant as a function of temperature and (b) a PFM phase image obtained with an external electrical field of 2500 V/cm [27].

constant at 50 kHz as a function of temperature for crystalline GST films quoted from Reference 27. The dielectric constant increases abruptly about 4–6 times with a maximum at $T_c$ = 259 ℃. In addition, the reciprocal dielectric constant shows a typical Curie–Weiss behavior for temperatures above $T_c$ as shown in the inset figure. Figure 3.9 (b) shows ferroelectric domains of FCC GST films quoted from Reference 27. With an external electrical field, ferroelectric domains are observed in PFM phase images. Bright and dark areas correspond to the ferroelectric domains which have opposite orientation. The domain size ranges from 50 to 100 nm and increases as the external electric field increases. In HCP phase ferroelectric domains disappear. To increase the memory window of a ferroelectric memory, one employs a ferroelectric with high remnant polarization and low dielectric constant. Most inorganic ferroelectric materials, however, have high dielectric constants. Ferroelectric polymers, not quite suitable for mainstream silicon technology, do have low dielectric constants

[79]. GST, because of its uniqueness of low dielectric constant (~40) and technology compatibility, is therefore of unique interest.

### 3.2.2 Resistance as a function of temperature

While the deposited sputtered GST film may be amorphous or micro-crystalline, due to the temperatures and durations of fabrication processes (oxide deposition, PR ashing, contact annealing, etc), the post-processed structure of GST becomes polycrystalline. That is, after the fabrication process is completed, the phase of GST has changed to the FCC phase as shown in Figure 3.10. It can be understood from the fact that the thermal budget of the fabrication process is around 200 ℃, 10 min. The temperature dependence of the film resistance in FCC and HCP phases are different. Prior to 300 ℃ annealing, the phase is FCC, and following it, HCP. FCC

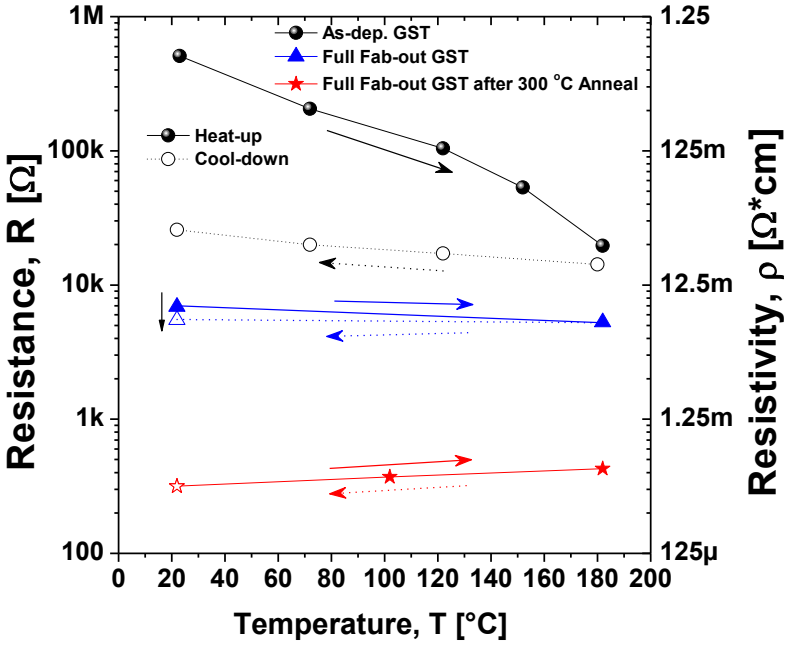



**Figure 3.10** Temperature dependence of GST film resistivity for different processing conditions.

phase has a negative temperature dependence of resistivity while HCP is positive one. This implies that in order to keep the phase in the FCC crystalline, the temperature of the fabrication process should not be above 250 ℃ of the transition temperature from FCC to HCP.

## *3.3 Samarium Nickelate, $SmNiO_3$*

### 3.3.1 Transition mechanism and physical properties of SNO

Rare-earth nickelates $R\mathrm{NiO_3}$ ($R$ stands for rare-earth elements such as Pr, Nd, and Sm), have been studied in recent years due to their metal-insulator phase transition (MIT) as a function of temperature [80]–[83]. The inherent electronic phase transition is of interest for applications in electronic and optoelectronic switches and memory devices [84]. The $R\mathrm{NiO_3}$ compounds are representative correlated electron systems and have distorted perovskite structures as shown in Figure 3.11 (a). At high temperature, they are metallic with orthorhombic symmetry [85], [86]. As temperature decreases, charge disproportionation occurs between Ni sites ($2\mathrm{Ni}^{3+} \rightarrow \mathrm{Ni}^{3+\delta} + \mathrm{Ni}^{3-\delta}$), reducing the symmetry to monoclinic and resulting in a transition to an insulating state [87]. The exact nature (i.e. charge order, Mott, etc.) of the insulating state has not been well understood, but the change in resistivity can be several orders of magnitude. The crystal distortion from ideal perovskite is quantified by Ni–O–Ni bond angle related to the radius of a rare-earth cation [80, 85]. Ideal perovskite has 180° of Ni–O–Ni bond angle. With the increase of atomic number and hence the decrease of the radius of a rare-earth cation, Ni–O–Ni bond angle decreases and hence the structure is distorted more severely. This distortion affects the critical temperature of the phase transition

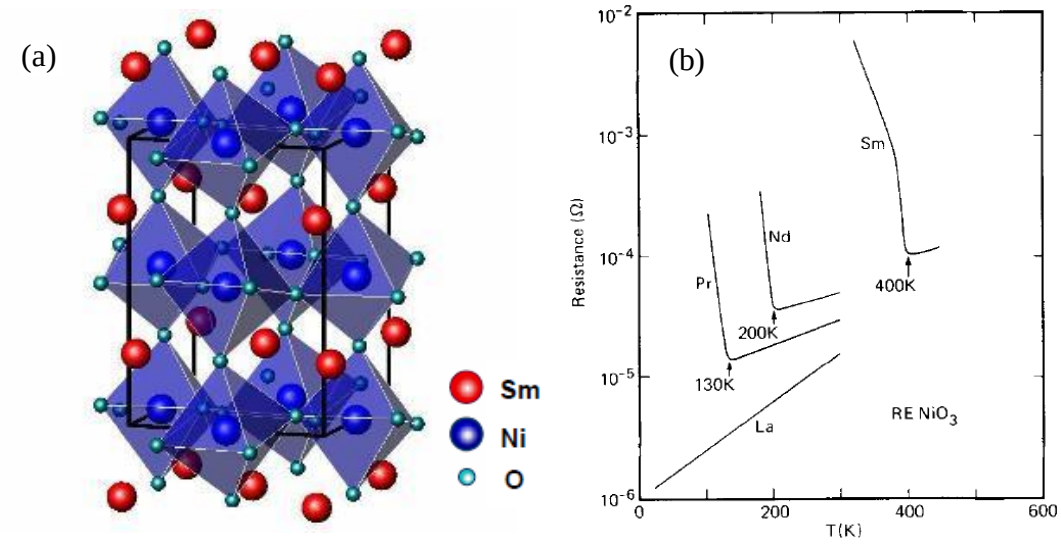



**Figure 3.11** (a) Crystal structure of SNO and (b) resistances as a function of temperature of several rare-earth nickelates [80].

[85]. As temperature increases, the distortion of a rare-earth nickelate reduces and its resistance decreases. In addition, the transition temperature is a function of the size of a rare-earth cation with smaller rare-earth cation causing greater distortion of the perovskite unit cell and therefore, higher temperature is needed to reduce the distortion and lift the charge disproportionation. Therefore, the most distorted one has the highest transition temperature as shown in Figure 3.11 (b). $SmNiO_3$ (SNO) is of particular interest among the $RNiO_3$ because it is the first in the series with MIT temperature above room temperature (~400 K in the bulk) [88].

Owing to the instability of 3+ oxidation state of Ni, oxygen vacancies are present in a SNO film [83], [85]. It is known that these oxygen vacancies can modify the phase transition properties [85]. In addition, they lead to space charge creation and influence the conduction properties of SNO thin films. Especially, at high field, it has been observed that space charge limited current is dominant [83]. Space charge can

affect the dielectric property of a SNO film. Nevertheless, the dielectric property of SNO has not been studied intensively so far.

### 3.3.2 Crystalline Phase and Surface Morphology Analysis

The SNO film is deposited by rf magnetron sputtering from a 99.99 % pure ceramic target in an $Ar/O_2$ mixture with the substrate held at 650 °C. To confirm the crystalline phase of the SNO film, X-ray diffraction (XRD) analysis is performed. Thermally-induced metal-insulator phase transition property is also directly measured through in-plane conductivity measurement. As shown in Figure 3.12 (a), there are several $SmNiO_3$ peaks as well as other peaks from binary $NiO_x$ and $SmO_x$ phases. Note that it is common for some of the transition metal-oxides to have mixed phases when they are grown on non-lattice-matched substrates. This is in part due to the instability of the $Ni^{3+}$ valence state [89]. Although the SNO film used in the experiment is not a single phase SNO film, the film has a temperature-mediated

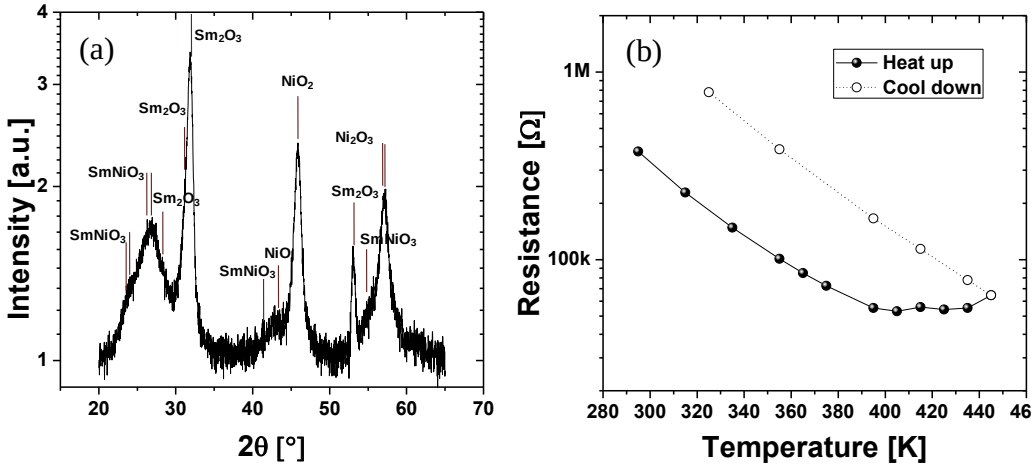



**Figure 3.12** Crystalline phase investigation of a SNO film: (a) Representative 2θ–ω scan of XRD analysis and (b) resistance vs temperature correlation plot.

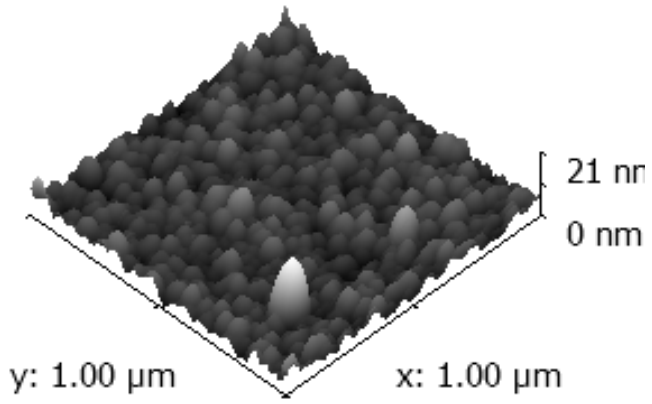



**Figure 3.13** Surface morphology and roughness of a SNO film examined by AFM.

transition property as shown in Figure 3.12 (b). The phase transition occurs at around 130 ℃, which is the typical phase transition temperature of bulk SNO. This implies that $SmNiO_3$ phase dominates other phases in the film.

The surface morphology and roughness of the SNO film are examined using an Atomic Force Microscope (AFM) as shown in Figure 3.13. On a 1 µm x 1 µm scanning area, the average roughness ($R_a$) and root mean square (RMS) roughness are 1.32 and 1.88 nm, respectively, which are 0.66 and 0.94 % of the thickness of the SNO film. This roughness value is sufficiently smooth for the film to be used as a gate insulator considering the fact that the roughness of an amorphous silicon film deposited by plasma enhanced chemical vapor deposition (PECVD) as a floating gate layer is ~2 nm [68].

## *3.4 Summary*

The transition mechanisms and physical properties of the phase transition materials used in the experiment have been discussed. The metal-insulator phase

transition of $VO_2$ can be induced not only by a thermal excitation, but also by photonic excitation or a high electric field. In the metallic phase, $VO_2$ has a tetragonal rutile structure with an octahedral symmetry. As the temperature decreases, the structure distorts and becomes monoclinic. The insulating $VO_2$ has about 0.7 eV band gap formed at the Fermi level between bonding $d_{\|}$ and the $\pi$ bands. Owing to the various oxidation states of vanadium, the vanadium oxide film in our experiments is composed of the family of various vanadium oxides. Although the atomic composition ratio acquired from the XPS analysis is not exactly 2, the film has a typical thermal hysteresis behavior of $VO_2$. Grain size of the $VO_2$ film is about 100 ~ 500 nm and its surface roughness is ~20 nm. Due to the off-centered displacement of vanadium cation, $VO_2$ is a ferroelectric material like $V_2O_5$.

GST has a structural transformation by a thermal or photonic excitation. GST undergoes two structural phase transitions: amorphous-to-FCC lattice at ~150 ℃ and FCC-to-HCP lattice at ~250 ℃. Localized structural transformation model presented by Kolobov et al. provides a clear explanation for the unusual band gap change and ferroelectricity of GST as well as the phase transition mechanism. GST is a ferroelectric material with the Curie temperature of 256 ℃. The post-processed GST is FCC crystalline owing to the thermal budget of the fabrication process.

SNO possesses the thermally-driven metal insulator phase transition property with a distorted perovskite structure. With smaller rare-earth cation causing greater distortion of the perovskite unit cell, the transition temperature should be higher. Due to the instability of 3+ oxidation state of Ni, oxygen vacancies appear and lead to space charge creation. There are other peaks from binary $NiO_x$ and $SmO_x$ phases as

well as $SmNiO_3$ peaks, but the film has a temperature-mediated transition property with the typical phase transition temperature of bulk SNO. The roughness is below 2 nm and thus the SNO film is sufficiently smooth to be used as a gate insulator.

# Chapter 4

# FABRICATION OF PHASE TRANSITION MEMORIES

This chapter describes the fabrications of phase transition memories: bulk-type devices with silicon substrates and suspended channel devices with SOI substrates. A conventional CMOS technology process is adopted and i-line lithography is used for photo-patterning. The device structure employs a gate composite of metal–insulator–phase transition material–insulator–semiconductor with the phase transition material as an intermediate gate insulator. In addition to memory transistors with the size splits of gate width and length, test element group (TEG) is designed to measure sheet resistance, contact resistance and gate field effect.

## *4.1 Fabrication of Bulk-type Phase Transition Memories*

### 4.1.1 Process flow

Using a 4 inch p-type silicon <100> wafer whose resistivity is 1 ~ 10 Ω·cm, bulk-type devices are fabricated. Figure 4.1 shows the schematic view of a MOSFET device of phase transition memory. The MOSFET structure is similar to that of a Flash memory and composed of a transistor with a phase transition material employed as an intermediate gate insulator. The phase transition material film is sandwiched between thermal $SiO_2$ and ALD $SiO_2$ layers on a p-type silicon substrate. $VO_2$, GST and SNO are used as phase transition materials in the experiment.

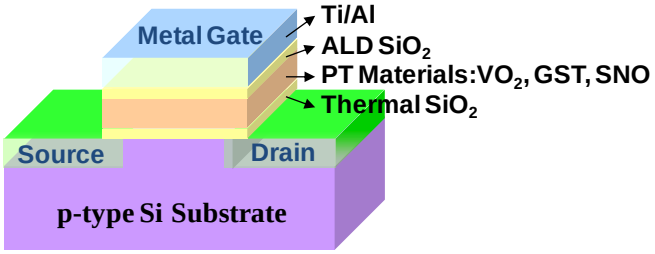



**Figure 4.1** Schematic view of a MOSFET structure with a phase transition film as a gate insulator sandwiched between silicon dioxide layers.

Fabrication sequences for a MOSFET device are illustrated in the Figure 4.2. In the beginning, alignment keys are formed on a wafer and then active area is defined by i-line lithography and a local oxidation of silicon (LOCOS) process. The GCA Autostep 200 is used as a photolithography tool and has an Olympus 2145 (N.A. =

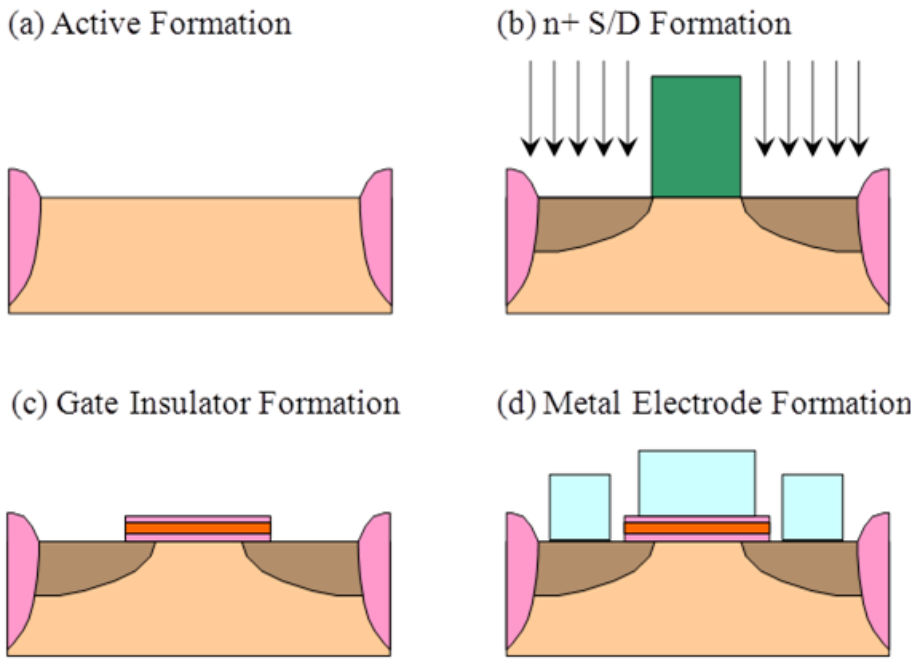



**Figure 4.2** Fabrication sequences for a MOSFET device: (a) Active regions formed by LOCOS process, (b) n+ S/D regions formed by As IIP, (c) gate insulator patterns formed by several dry etch steps, and (d) gate and S/D metal electrodes formed by lift-off processes.

0.45) lens that reduces the mask image by 5X and gives a resolution of ~0.5 μm in the center of the lens field. The system can produce 0.5 um isolated patterns using a wafer auto-leveling system that works for wafers and pieces. In case of the manual alignment using global alignment keys, misalignment better than 0.25 μm is achievable. Using the micro-DFAS local alignment system, alignment error reduces to 0.10 μm. With the 700 W Hg arc lamp, the light intensity of ~475 mW/cm² can be applied to the wafer. For the LOCOS process, a 100 nm silicon nitride film is deposited on a sacrificial silicon dioxide layer. After the active areas are defined, a wet oxidation is performed at 1100 ℃ for 40 minutes growing a 500 nm silicon dioxide layer on field areas. A 40 keV boron implantation for channel doping is performed at a dose of $2x10^{12}$ $cm^{-2}$. After photo-patterning, a 30 keV arsenic implantation is performed at a dose of 3 x $10^{15}$ $cm^{-2}$ to define S/D regions. After doing a rapid thermal annealing (RTA) process at 1000 ℃ for 10 seconds to activate the ion-implanted dopants, thermal $SiO_2$ (20 nm) is grown at 1000 ℃ for 10 minutes, followed by the deposition of a phase transition film and a 110 ℃ plasma atomic layer deposition (ALD) process for the growth of a $SiO_2$ layer (50 nm). In the experiment, $VO_2$, GST and SNO films are used as phase transition layers. The $VO_2$ film is deposited with a DC reactive sputtering process in Ar (91.2 %) + $O_2$ (8.8 %) environment at 10 mTorr from a V target. The base pressure in the sputtering chamber is $2 \times 10^{-8}$ Torr and the substrate temperature is kept at 550 ℃ during the deposition. The GST film is formed via rf sputtering. The SNO film is deposited by rf magnetron sputtering from a 99.99% pure ceramic target in an $Ar/O_2$ mixture with the substrate held at 650 ℃. For the S/D contacts, $CHF_3/O_2$ is used to etch the $SiO_2$ layers and $CF_4$ for $VO_2$, $CHF_3/O_2$ for GST

and ion miller for SNO are used to etch the films. 50 nm Ti and 300 nm Al are evaporated for the lift-off process of gate and S/D electrodes. In case of S/D electrodes, a wet etching process is done using a 6:1 buffered oxide etchant before Ti and Al evaporations.

### 4.1.2 Gate insulator patterning process

A 200nm $VO_2$ film is deposited on a bottom gate insulator of thermal silicon dioxide. Then, a top gate insulator of silicon dioxide is deposited on the $VO_2$ film by 500 plasma ALD cycles at 110 ℃. After photo-patterning, reactive ion etching (RIE) process using an Oxford PlasmaLab 80 etcher is performed to form a gate insulator pattern that is 2 μm per side larger than a related gate pattern to obtain a misalignment margin. RIE process consists of 2 steps. The $1^{st}$ step is to etch the bottom silicon dioxide by a $CHF_3/O_2$ recipe ($CHF_3$ 50 sccm, $O_2$ 2 sccm, 50 mT, 200 W), the etch rate (E/R) of which is about 30 nm/min for $SiO_2$. The $2^{nd}$ step is to etch the $VO_2$ film by a $CF_4$ recipe ($CF_4$ 30 sccm, 40 mT, 150 W), the E/R of which is about 400 nm/min for $VO_2$. Each step has an $O_2$ plasma pretreatment before main etching process to remove the residue of photo resist (PR) or polymer.

For GST devices, a 150 nm GST film is deposited. RIE process consists of just one step. The $CHF_3/O_2$ recipe is used and its E/R for GST is about 100 nm/min. For SNO devices, a 200nm SNO film is deposited. After photo-patterning, Ar sputter-etching process using a Vecco ion milling system is performed to form a gate insulator pattern. A 10 cm Kaufman Argon Ion beam source is used to sputter-etch materials up to 4 inch diameter. Typical parameters for ion milling are as follows: Beam voltage is

500 V, suppressor voltage is 200 V, discharge voltage is 40 V, chamber pressure is 1.5 x $10^{-5}$ Torr, beam current is around 80 mA, rotation speed is 3 rpm and tilt angle is 10°. Etching process consists of 2 steps. The 1st step is to etch the bottom silicon dioxide by the $CHF_3/O_2$ recipe. The 2nd step is to etch the SNO film by ion milling, the E/R of which is around 15 nm/min for SNO and around 50 nm/min for PR.

### 4.1.3 TEG description

In order to measure contact resistance ($R_c$), sheet resistance ($R_{sh}$) and gate field effect, test elements are designed. Figure 4.3 shows the test patterns for the measurement of contact resistance between metal and under layer. One is for the measurement of area contact resistance and the other is for the measurement of side contact resistance. When current flows between pad 1 and 2, potential difference between pad 3 and 4 generates due to the contact resistance. Thus, through the measurement of voltage difference between pad 3 and 4, the contact resistance can be extracted using Ohm's law as follows.

$$R_c = \frac{V_{34}}{I_{12}}, \tag{4.1}$$

where $I_{12}$ is the forcing current flowing between pad 1 and 2 and $V_{34}$ is the voltage difference between pad 3 and 4. Figure 4.4 shows the test patterns for the measurement of both contact and sheet resistances. One has area contacts between metal and under layer and the other has the side contacts. Through the current-voltage measurement between any two pads, total resistance ($R_T$) can be easily extracted. The total current is composed of the sheet resistance ($\rho_s$) of bottom layer and the contact

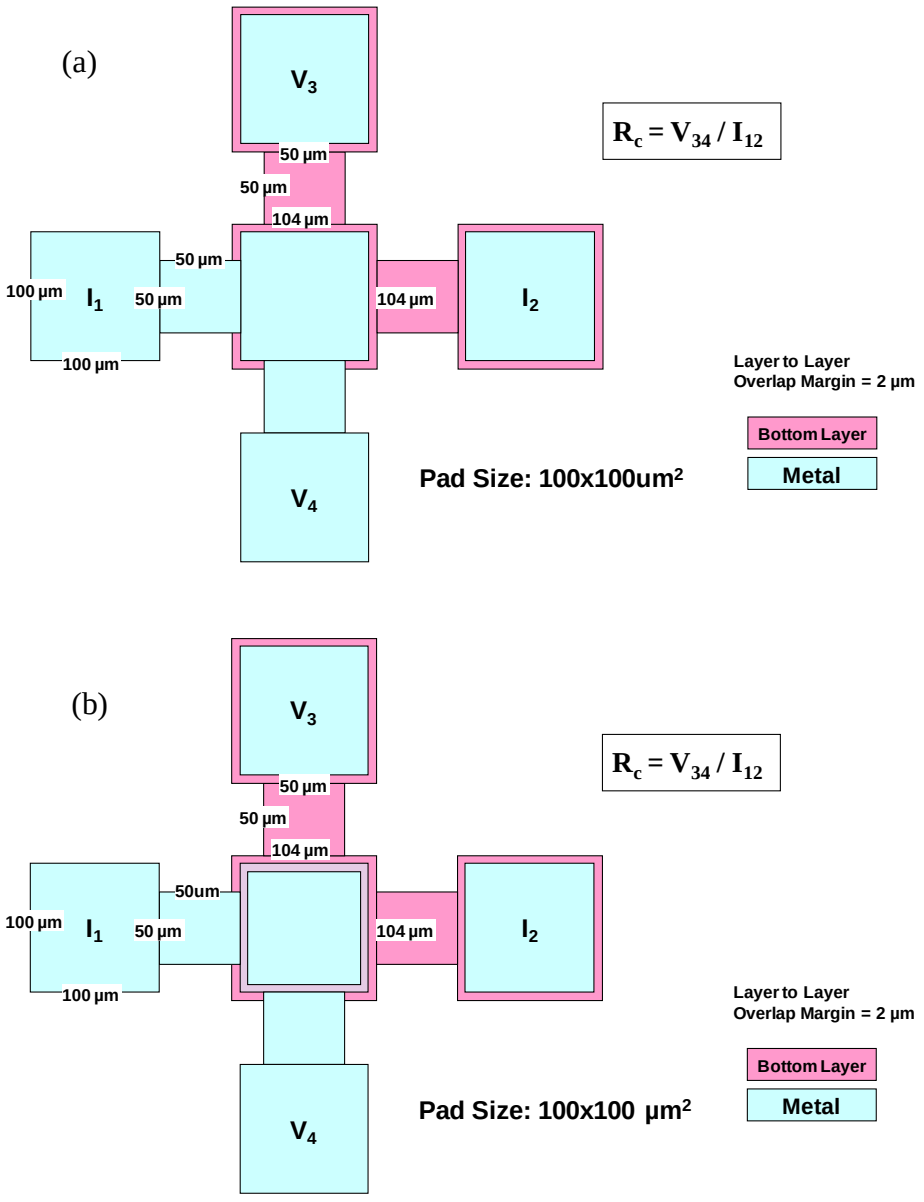



**Figure 4.3** Test elements for the measurement of contact resistance: (a) Test pattern for area contact resistance and (b) test pattern for side contact resistance.

resistance between metal and bottom layer and is correlated with them like this equation.

$$R_T = 2R_c + \left(\frac{\rho_s}{Z}\right) \times d\ , \tag{4.2}$$

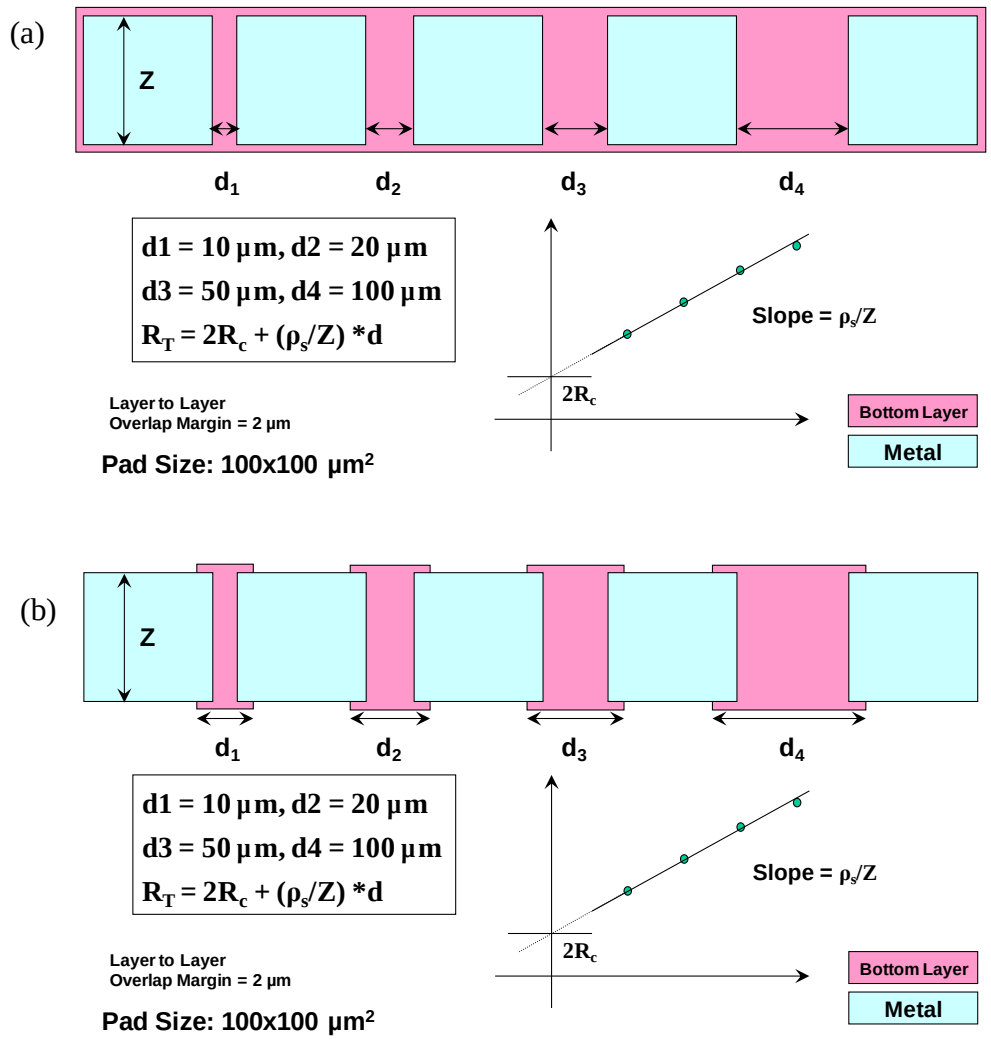



**Figure 4.4** Test elements for the measurement of both contact and sheet resistances: (a) Test pattern for area contact and (b) test pattern for side contact.

where $Z$ is the width of the pad and $d$ is the space between two pads. Therefore, contact and sheet resistances can be extracted from the extrapolation of measured total resistances data as shown in Figure 4.4. The contact resistance is half of y-intercept of an extrapolated line from the correlation between $R_T$ and $d$ and the sheet resistance is $Z$ times the slope of the line. The sheet resistance can be extracted from the measurement of a test element shown in Figure 4.5 (a). This test pattern looks like a

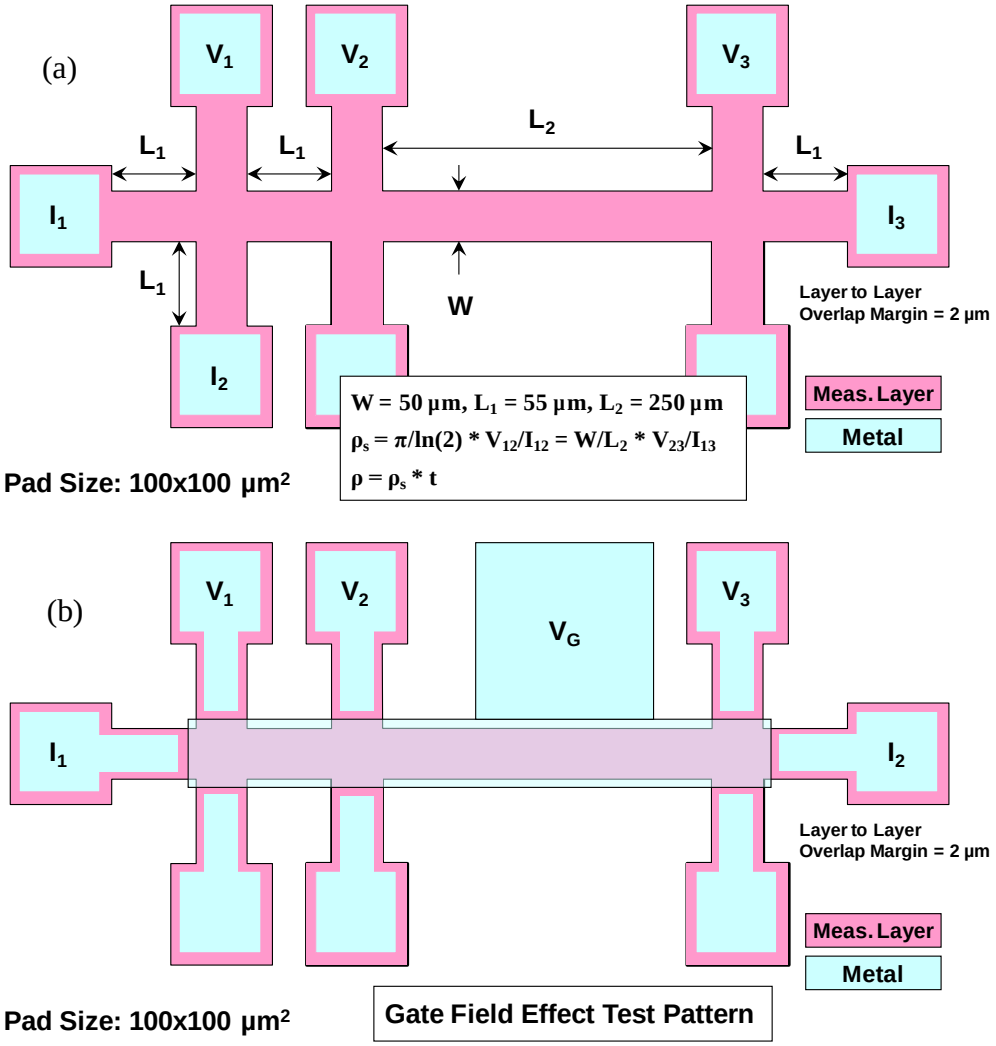



**Figure 4.5** Test elements for the measurement of sheet resistances: (a) Test pattern for sheet resistance and (b) test pattern for gate field effect on resistance.

Hall bar geometry. So, the mobility of a film can be measured with this element. First, using $I_1$, $I_2$, $V_1$ and $V_2$ pads, the sheet resistance can be extracted from the van der Pauw formula as follows.

$$\rho_s = \frac{\pi}{\ln(2)} \times \frac{V_{12}}{I_{12}}, \tag{4.3}$$

where $I_{12}$ is the forcing current flowing between $I_1$ and $I_2$ pads and $V_{12}$ is the voltage difference between $V_1$ and $V_2$ pads. Secondly, using $I_1$, $I_3$, $V_2$ and $V_4$ pads, the sheet resistance can be extracted from this equation.

$$\rho_s = \frac{W}{L_2} \times \frac{V_{23}}{I_{13}}, \tag{4.3}$$

where $I_{13}$ is the forcing current flowing between $I_1$ and $I_3$ pads and $V_{23}$ is the voltage difference between $V_2$ and $V_3$ pads. Figure 4.5 (b) shows a test element to measure the gate field effect on the resistance of a film. This element is designed to verify the phase transition of a phase transition material induced by the electric field.

## *4.2 Fabrication of Suspended Channel Phase Transition Memories (SCPTM)*

### 4.2.1 Process flow

For the improvement of heat delivery efficiency, which was defined in Chapter 2, a suspended channel device is proposed. Figure 4.6 shows the schematics of a suspended channel transistor. This is a new transistor with a wire based structure with air-gap under the channel. The air-gap is adopted to decrease heat conduction delivered from the channel downwardly resulting in efficient heat delivery to a phase transition material. Thermal conductivity of air is 0.025 W/mK, which is 6000 times smaller than that of silicon. More details about heat delivery efficiency will be discussed in Chapter 6. To make suspended channel devices, 4 inch p-type SOI wafers are employed. The thicknesses of buried oxide and top silicon are 400 and 340 nm,

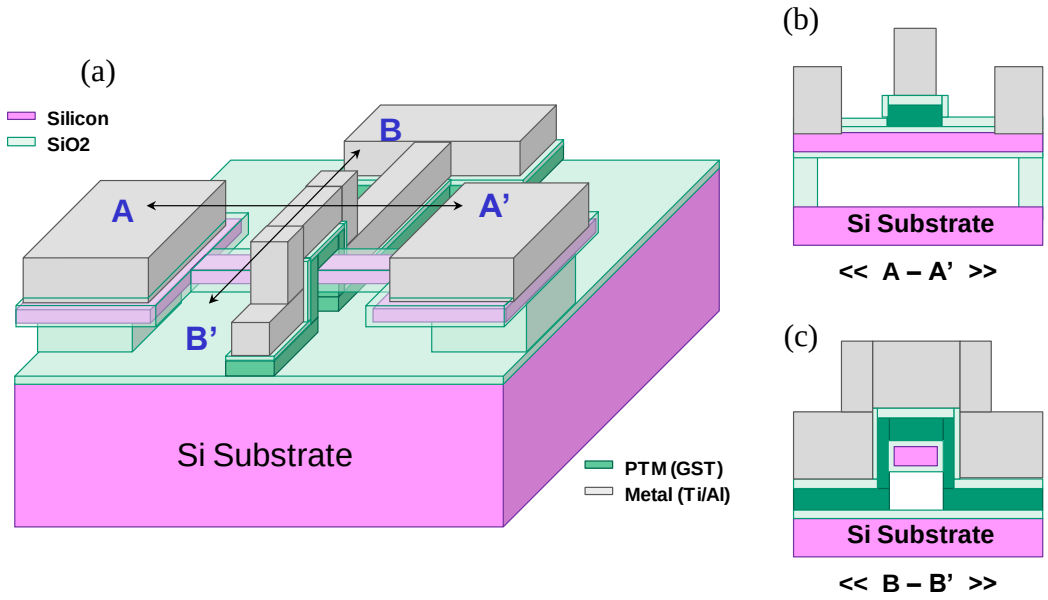



**Figure 4.6** Schematics of a suspended channel transistor: (a) 3D schematic view, (b) A–A' cross section view and (c) B–B' cross section view.

respectively, the crystal orientation of top silicon is <100>, and the resistivity is 14 ~ 22 Ω·cm.

Fabrication sequences for a SCPTM are illustrated in the Figure 4.7. Like the bulk-type PTM device, the GCA Autostep 200 is used for a photolithography tool. For the formation of alignment marks, multi-step RIE process is needed. The 1$^{st}$ step is to etch the sacrificial silicon dioxide by a $CHF_3/O_2$ recipe ($CHF_3$ 50 sccm, $O_2$ 2 sccm, 50 mT, 200 W). The 2$^{nd}$ step is to etch the top silicon layer by a $SF_6/O_2$ recipe ($SF_6$ 30 sccm, $O_2$ 10 sccm, 200 mT, 200 W), the E/R of which is about 1500 nm/min for Si. The 3$^{rd}$ step is to etch the buried oxide by the $CHF_3/O_2$ recipe and the 4$^{th}$ step is to etch the remaining oxide and silicon substrate by a $CF_4$ recipe ($CF_4$ 30 sccm, 40 mT, 150 W), the E/R of which is about 30 nm/min for $SiO_2$ and 60 nm/min for Si. The final step is to etch the silicon substrate by the $SF_6/O_2$ recipe. For active patterning,

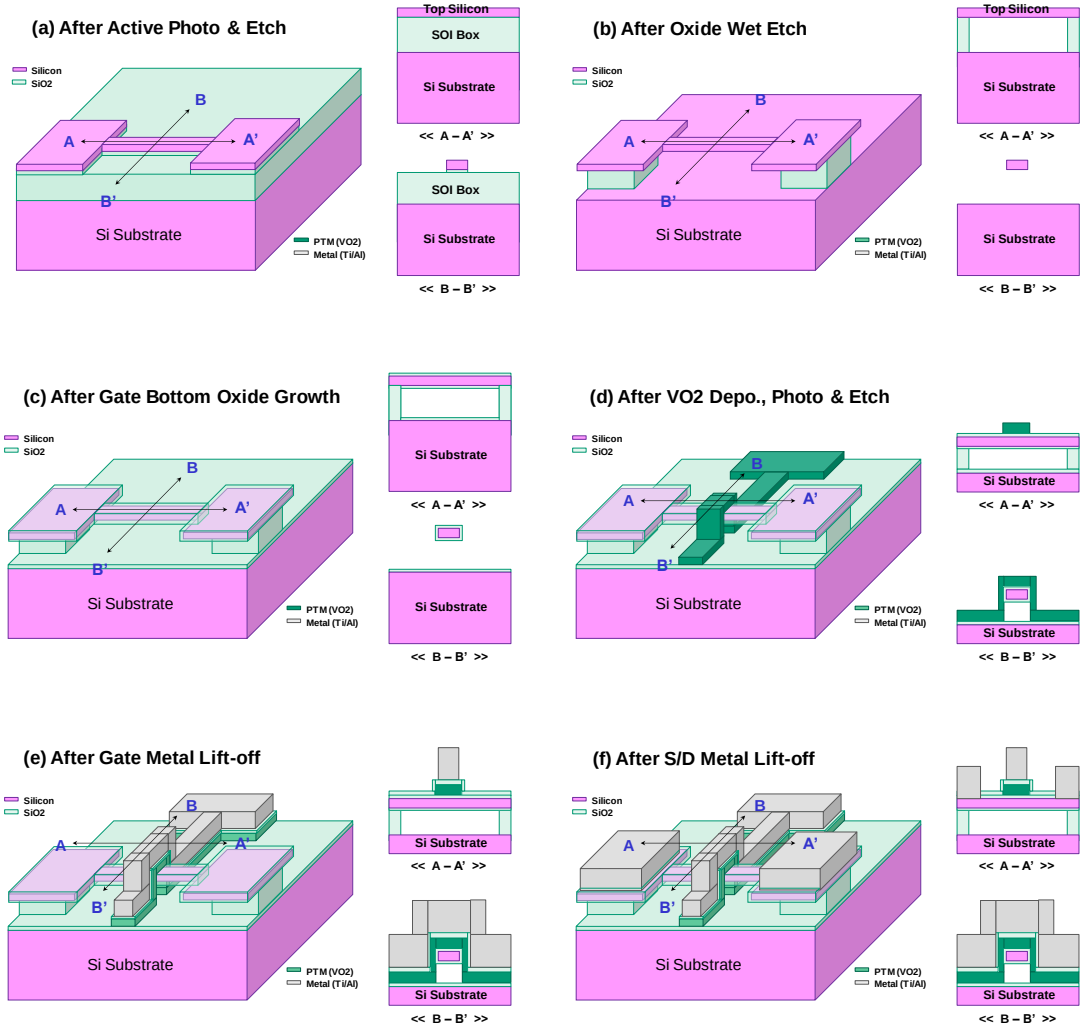



**Figure 4.7** Process flow of a suspended channel transistor.

LOCOS process is not needed because of the use of SOI wafers. After the active areas are defined, a 25 keV arsenic implantation for S/D doping is performed at a dose of 1 x $10^{15}$ $cm^{-2}$ on S/D regions defined by photo-patterning. After doing a rapid thermal annealing (RTA) process at 1000 ℃ for 10 seconds to activate the ion-implanted dopants, 30 nm ALD silicon dioxide and 150 nm silicon nitride films are deposited for the removal of buried oxide under the channel. After the channel open process

composed of a photo-patterning and RIE, a selective wet etch process is employed. Except the thickness of gate metal, the remaining fabrication process is the same as that of the bulk-type device. The gate metal consists of 50 nm Ti and 600 nm Al to prevent the breakage of the metal line at the sidewall of the channel.

### 4.2.2 Selective wet etching process for the air-gap

The suspended channel device has an air-gap under the channel. The air-gap is formed by a selective wet etching process. In the process, it is a critical factor to prevent direct contact between the channel and substrate caused by unwanted silicon bending. Thus, a channel open mask, the patterns of which are locally open in the channel area of devices is adopted to minimize the removal of buried oxide in the region without the channel. Figure 4.8 shows the examples of channel open patterns. A 30 nm ALD silicon dioxide layer is deposited as an etch stopper and stress reliever

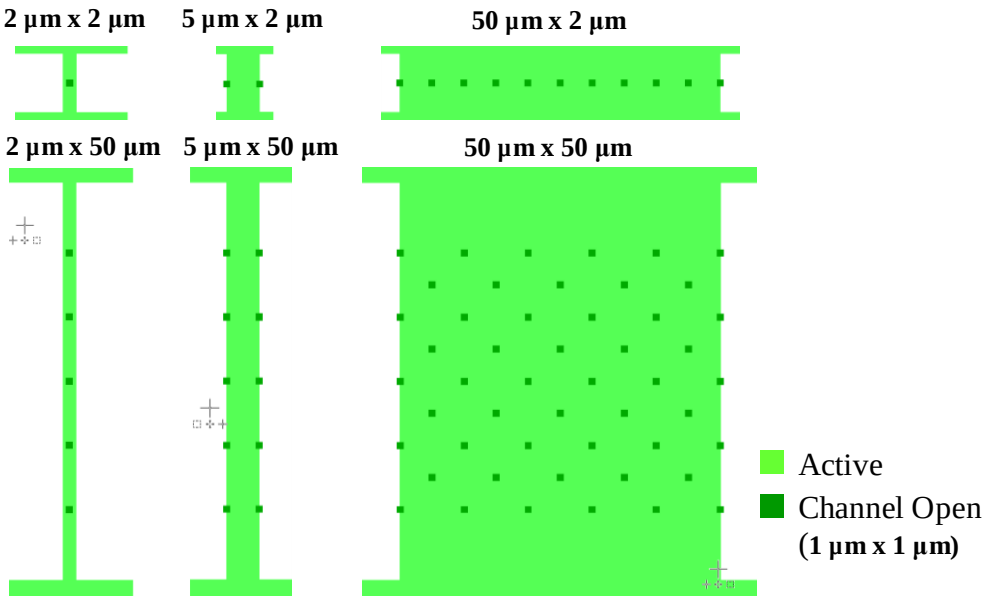



**Figure 4.8** Examples of channel open patterns for the air-gap under the channel.

created between the silicon and nitride layer. Then, a 150 nm silicon nitride film is deposited as a wet etch mask to realize the selective wet etching. After photo-patterning, a RIE using a $SF_6/O_2$ recipe ($SF_6$ 30 sccm, O2 10 sccm, 200 mT, 200 W) is proceeded to remove the silicon nitride film and hence open the channel region. Its E/R is about 140 nm/min for silicon nitride. After that, a wet etching step is performed. An aqueous hydrofluoric acid (49% HF) is used as a wet etch chemical. 49% HF can get rid of silicon dioxide at the rate of 1,800 nm/min, which is more than 100 times faster than the etch rate of silicon nitride of 14 nm/min. Moreover, silicon is almost not etched by 49% HF. After removing the buried oxide, the silicon nitride film is striped by 160 ℃ phosphoric acid, the E/R of which is around 5 nm/min for silicon nitride.

## *4.3 Summary*

The fabrication processes of phase transition memory transistors have been reviewed. A conventional memory technology is employed for the fabrication and an i-line photolithography tool is adopted for photo-patterning. Bulk-type devices are made with p-type silicon wafers. Several test elements are designed to measure sheet resistance, contact resistance and gate field effect. To improve the heat delivery efficiency, a suspended channel phase transition memory is proposed and made with a p-type SOI wafer. The suspended channel device has an air-gap under the channel and unwanted silicon bending is the most critical issue in the process. More details on fabrication processes will be described in Appendix A.

# Chapter 5

# CHARACTERIZATION OF BULK-TYPE DEVICES

This chapter discusses the results of bulk-type phase transition memory transistors: $VO_2$, GST and SNO devices. Irrespective of phase transition materials, all devices have hysteresis properties in response to the gate voltage at room temperature. With the cycling of the gate voltage, gate capacitance and drain current cycle counterclockwise. This effect is opposite to the hysteretic phenomenon caused by charge trapping and consistent with the polarization switching effect. With only a gate pulse, the threshold voltage is modulated without any other biases at room temperature. Therefore, this is a gate field effect, not a thermally-induced phase transition effect. In case of $VO_2$ and GST, ferroelectric polarizations seem to be dominant considering that there are the displacements of cations (V cation for $VO_2$ and Ge cation for GST) in their crystal structures resulting in net dipole moments. On the other hand, space charge polarization is dominant in a SNO film that has non-negligible oxygen vacancies due to the instability of the $Ni^{3+}$ valence state. The devices are nonvolatile memories with the state retention times of the order of minutes due to the depolarization field that always exists owing to the finite dielectric constant of a semiconductor with the use of ferroelectric materials placed on a semiconductor.

## *5.1 $VO_2$ Devices*

### 5.1.1 Voltage hysteretic behaviors

Voltage hysteresis is a typical property of a memory device. The device with voltage hysteretic behaviors can be in more than one state at the same bias condition. That is, the device can store different information or one binary bit (0 or 1) in response to its operational history. Figure 5.1 shows the capacitance–voltage and current–

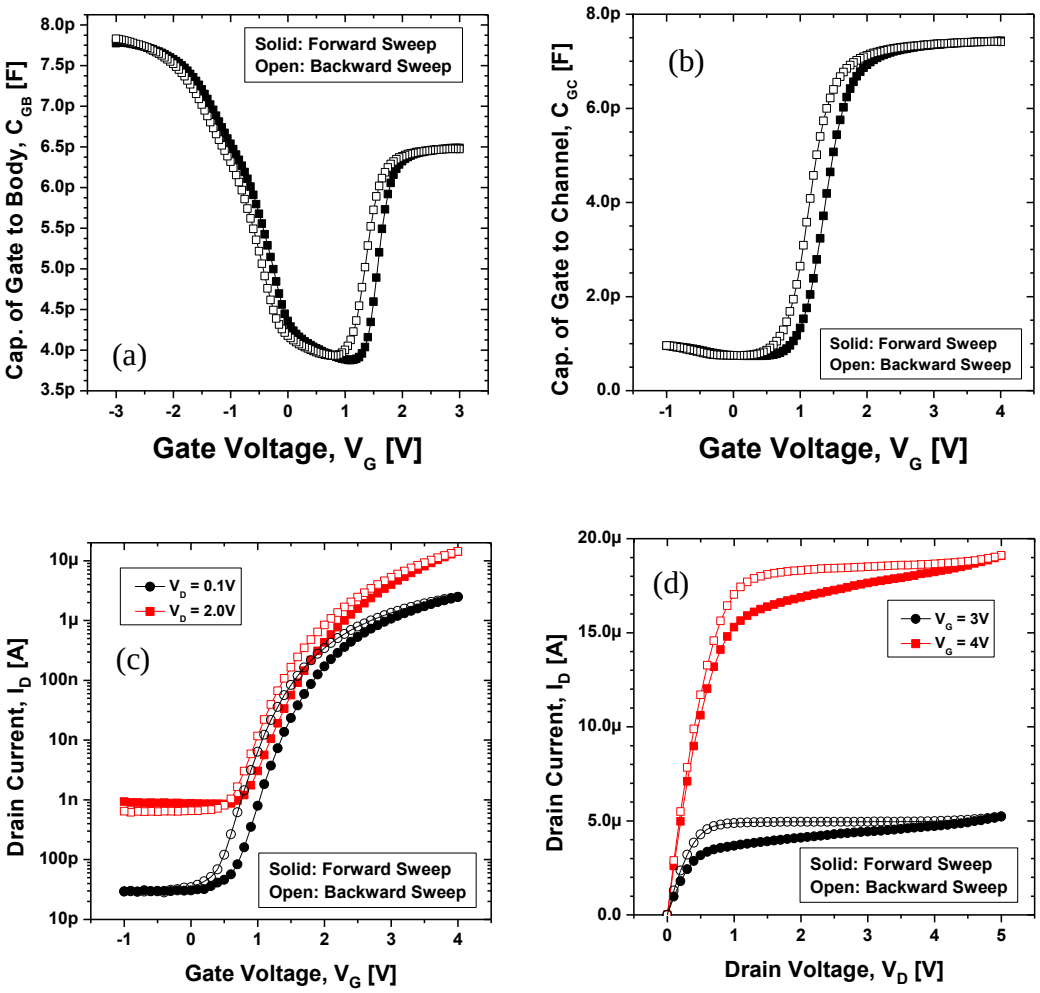



**Figure 5.1** Voltage hysteretic behaviors of (a) gate to body capacitance, (b) gate to channel capacitance, (c) drain current in response to gate voltage and (d) drain current in response to drain voltage.

voltage hysteretic behaviors of $VO_2$ transistors measured at room temperature. The device size is 100 µm x 100 µm (width x length). When the gate voltage sweeps backwardly after forward sweeping, the threshold voltage reduces and hence the drain current increases. Drain bias also affects the hysteresis characteristics because it changes the field across the transistor. Considering that it happens without drain current at room temperature, this hysteresis is not related to heat-triggered metal-insulator phase transition effect, but a gate field-induced effect. It is not caused by charge trapping since there is no charge injection and no current due to the thick $SiO_2$ layers in the capacitor structures.

The hysteresis still exists under the conditions of strong light intensity and higher temperature than the MIT temperature as shown in Figure 5.2. With the increase of light intensity, the threshold voltage decreases and the inversion capacitance increases. This is why the formation of inversion layers is accelerated by

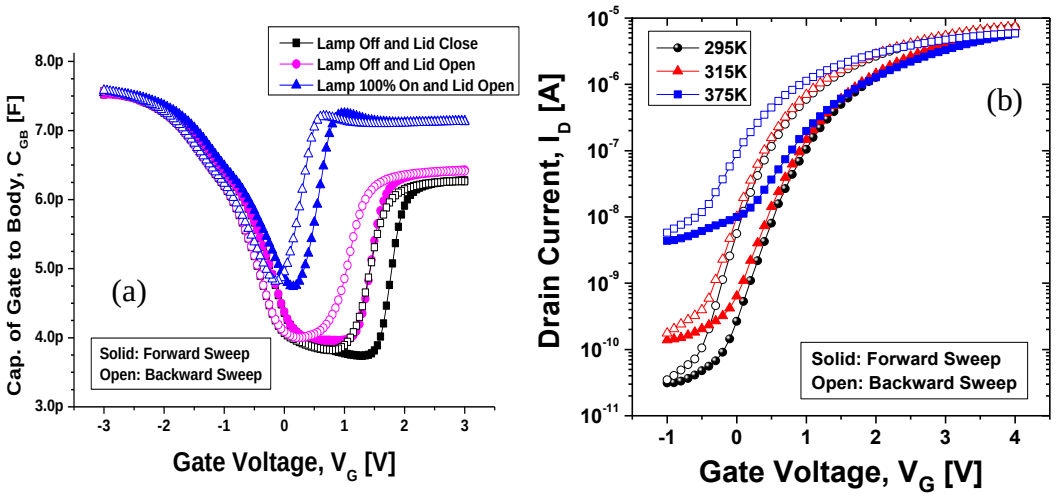



**Figure 5.2** Dependence of (a) capacitance-voltage hysteresis on light intensity and (b) current-voltage hysteresis on temperature.

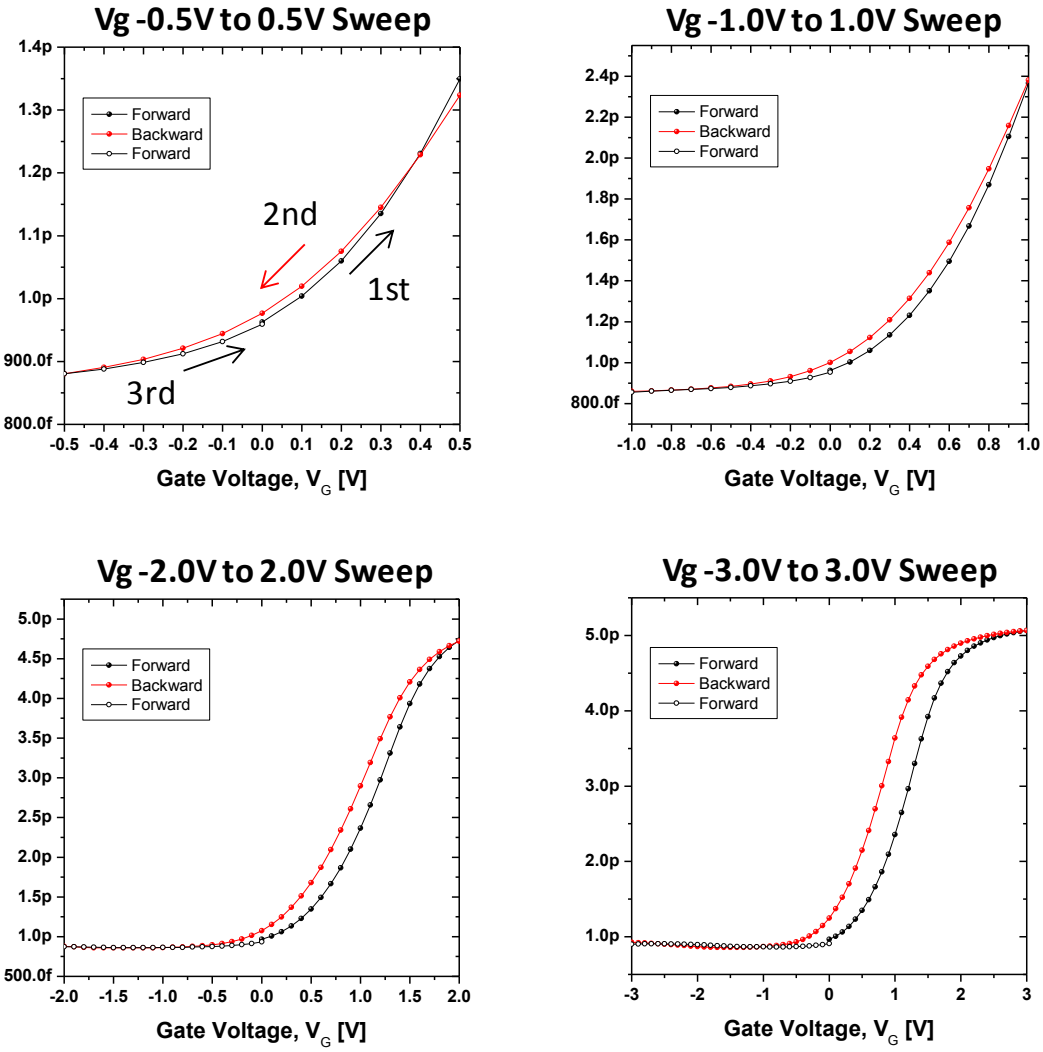



**Figure 5.3** Sweeping range dependence of capacitance-voltage hysteresis.

the increase of light intensity. As the temperature increases, the hysteresis window and Off-state current increase. The increase of Off-state current results from the increase of junction leakage current with temperature. More details about the temperature dependence of the hysteresis window will be discussed later.

Figure 5.3 shows the sweeping range dependence of capacitance-voltage hysteresis of a $VO_2$ device. As the sweeping range of the gate voltage increases, the

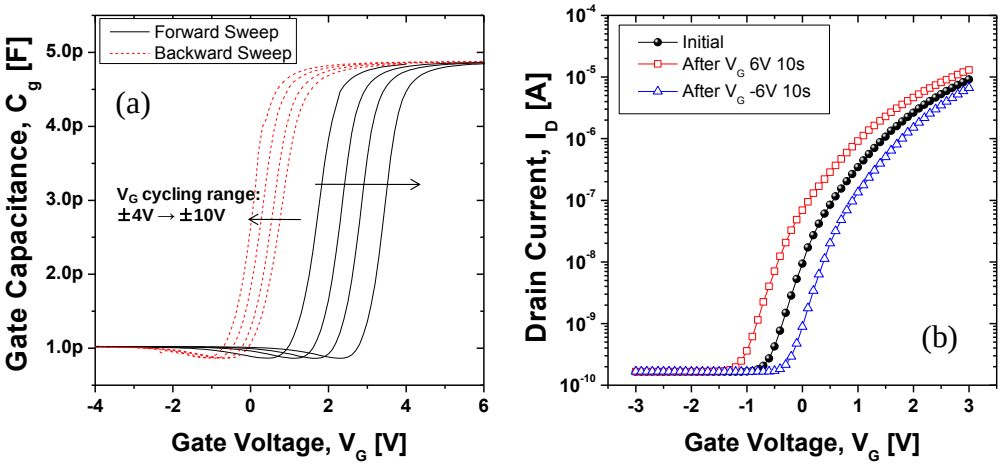



**Figure 5.4** Threshold voltage shift due to ferroelectric polarization switching: (a) Hysteresis behavior of gate capacitance in response to gate voltage and (b) Gate field dependency of threshold voltage shift.

hysteresis window increases. Even when the range reduces to 1 V (-0.5 to 0.5 V), the hysteresis does not disappear, which implies that this effect is very sensitive to the gate field. The gate voltage dependence of the hysteresis window is still effective at higher gate voltages as shown in Figure 5.4 (a). As the gate voltage is cycled between ±4, ±6, ±8, and ±10 V, the capacitance cycles counterclockwise (starting from negative voltage) and the memory window increases linearly according to the cycling range of the gate bias. In -4 to 4 V gate voltage cycling, the memory window of ~1 V is obtained. Figure 5.4 (b) shows the threshold voltage shift after gate pulsing without source and drain biasing. After applying the negative gate voltage, the threshold voltage shifts positively and vice versa. These shifts occur without channel current at room temperature, which indicates that this effect is independent of the phase transition of $VO_2$ film. These measurements, their existence at low temperatures, and their existence in the absence of heating, can be explained through postulating ferroelectric polarization mechanism in the $VO_2$ film.

### 5.1.2 Ferroelectric properties

As discussed in Chapter 3, $VO_2$ has a distorted rutile structure in which a vanadium ion has moved away from the center of an oxide octahedron. These off-centered displacements result in a net dipole moment, which suggests that $VO_2$ is a ferroelectric material. The hysteretic behaviors observed in the experiments are consistent with ferroelectric polarization switching and opposite of the hysteresis resulting from charge trapping in the gate insulators. This result is the first evidence to show the possibility that $VO_2$ can be ferroelectric in the memory structure fabricated in our experiments.

The remnant polarization of a ferroelectric material is one of the most important properties that determine the memory window of a ferroelectric memory device as described in Equation 1.2. Thus, to extract the remnant polarization of $VO_2$, the saturation phenomenon of threshold voltage shift was considered. Figure 5.5 (a) shows C-V curves at the various sweep ranges of gate voltage and Figure 5.5 (b)

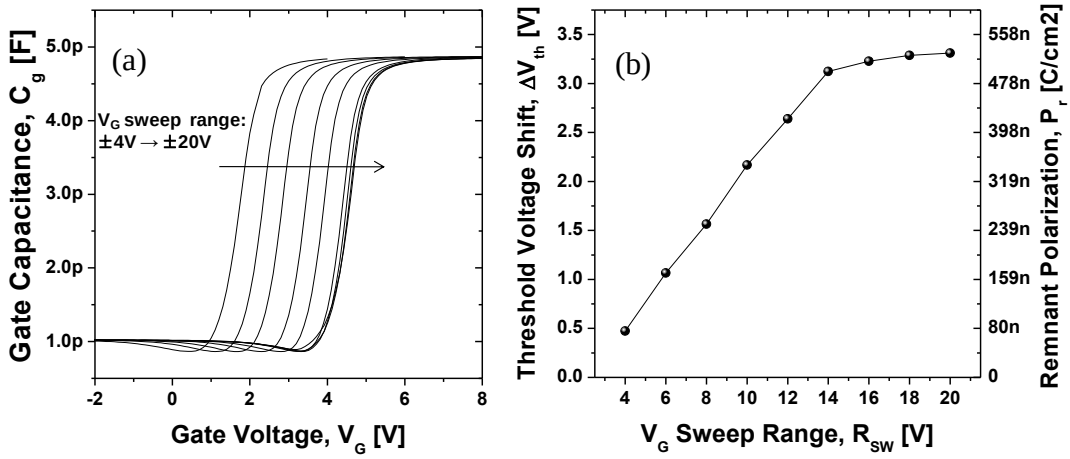



**Figure 5.5** Remnant polarization of $VO_2$: (a) C-V curves at various sweep ranges of gate voltage and (b) Trend of threshold voltage shift as a function of the sweep range.

shows the trend of threshold voltage shift as a function of the sweep range. As shown in these figures, the threshold voltage shift saturates as the sweep range of the gate bias reaches 20 V. This implies that the polarization of $VO_2$ saturates at 20 V and the $VO_2$ film has the remnant polarization when the gate field is removed. Therefore, using the Equation 1.2, one can extract the remnant polarization of $VO_2$ from the threshold voltage shift at the sweeping gate voltage of 20 V. This is ~0.53 μC/cm2. This value is comparable to the minimum polarization for the FeDRAM proposed by Prof. Ma [13].

After applying the saturation field to $VO_2$, the hysteresis behaviors of gate capacitance in response to gate voltage are observed to extract the coercive field of $VO_2$, which is another important property of a ferroelectric material. Figure 5.6 (a) shows C-V hysteresis behaviors at the various cycling ranges of gate voltage and Figure 5.6 (b) shows the trend of average gate voltage when the gate capacitance is 2 pF as a function of the cycling range. As shown in these figures, the average gate

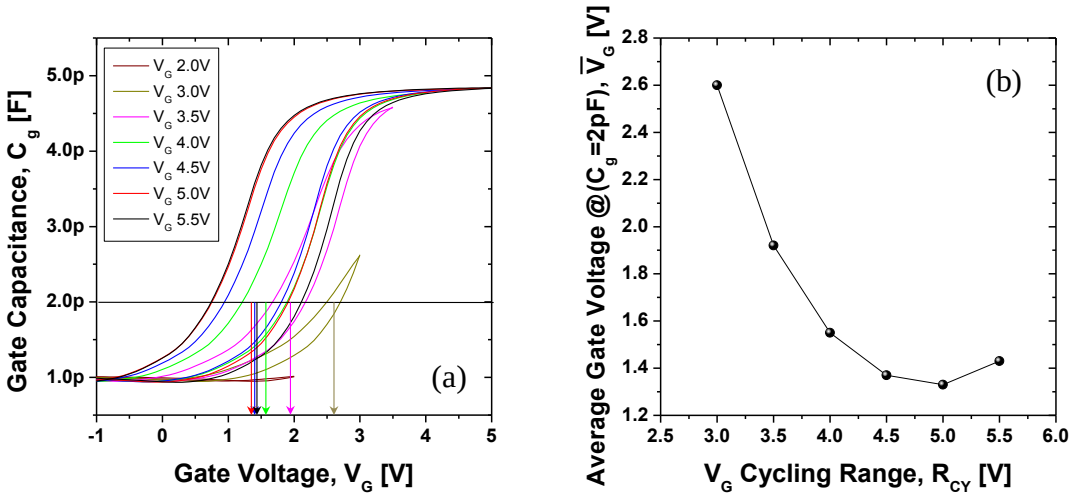



**Figure 5.6** Coercive field of $VO_2$: (a) C-V hysteresis at various cycling ranges of gate voltage and (b) Trend of average gate voltage when the gate capacitance is 2 pF as a function of the cycling range.

voltage of forward and backward sweeps saturated as the cycling range of gate bias reached 5 V. This means that when the field input to $VO_2$ is below the coercive field, the threshold voltage is still higher due to the remnant polarization, and when the field is over the coercive field, the average threshold voltage stabilizes because the remnant polarization is removed whenever the gate voltage is cycled. Therefore, when the gate voltage is 5 V, the coercive field is applied to the $VO_2$ film. Using the structural factors of the gate stack and the gate voltage, one can calculate the coercive field of $VO_2$. This is around 450 kV/cm2.

### 5.1.3 Data writing and retention characteristics

Figure 5.7 shows the data writing time of $VO_2$ devices. To measure the writing time, the increment of the capacitance as a function of gate pulse width is observed.

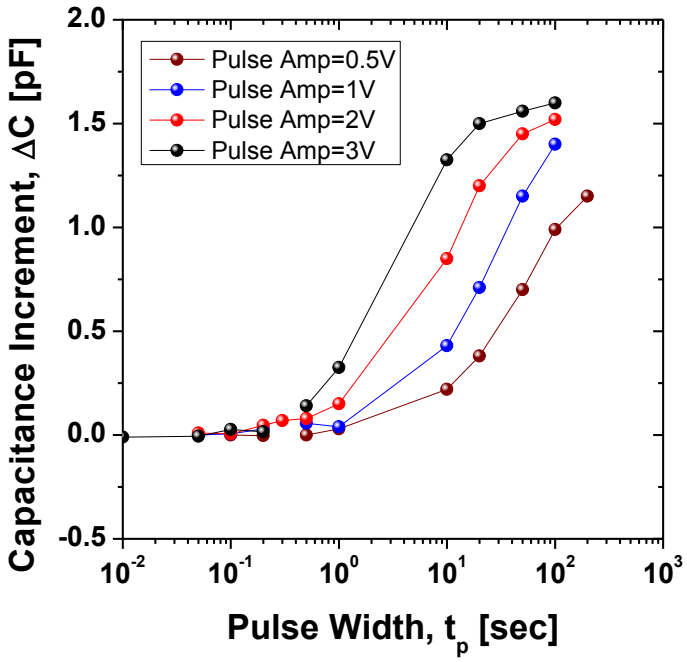



**Figure 5.7** Data writing characteristics: Increment of the capacitance as a function of gate pulse width is observed with several gate pulse voltages.

As shown in figure, data writing time is so slow compared to other memory devices. When the gate pulse amplitude is 3 V, the required writing time is above 0.1 msec. However, given the fact that the writing time reduces with the increase of the gate electric field and has the dependence of the devise size, the devices themselves are expected to be much faster. Ferroelectric transitions take place in nanoseconds and the smallest structure will have the writing time in nanoseconds.

When a ferroelectric material is inserted between metal plates, there is no depolarization field due to the charge compensation by image charges in the metal plates. On the other hand, in case of a ferroelectric field effect memory transistor, there exists a depolarization field ($E_{DP}$) due to the finite dielectric constant of a semiconductor:

$$E_{DP} = P_r / \left[ \kappa \varepsilon_o \left( \frac{C_S}{C_F} + 1 \right) \right], \tag{5.1}$$

where $C_S$ is the capacitance of a semiconductor film, and $C_F$, $P_r$ and $\kappa$ are the capacitance, the remnant polarization and the dielectric constant of a ferroelectric film, respectively [12].

Another factor affecting the retention characteristics is the charge injection to the gate dielectric stack. The trapped charges in the gate dielectric stack lead to local charge compensation and gradually deteriorate the polarization effect. The retention time determined by the charge injection is expected to be

$$t_{RET} = \frac{P_r}{I\alpha}, \tag{5.2}$$

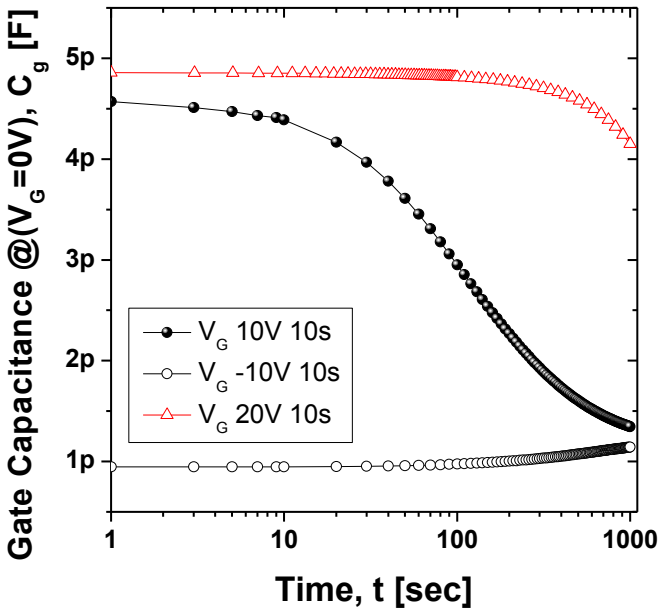



**Figure 5.8** Data retention time of a $VO_2$ memory device. In case of 20 V gate pulse, the retention time is around 15 minutes, which is three orders of magnitude longer than those of current generations of conventional DRAMs.

where $I$ is the gate leakage current and $\alpha$ is the trapping probability [12].

Due to the depolarization field and the charge injection, the polarization of the ferroelectric film disappears gradually and hence stored information decays. Figure 5.8 shows the data retention characteristics of implemented devices. To measure the retention time of $VO_2$ memory devices, the gate capacitance at zero gate bias is measured after applying a gate pulse to suppress data interference during the measurement. The retention time after a 10 V gate pulse is worse than after a 20 V gate pulse. This may be caused by the polarization instability of unsaturated ferroelectric film – the film is a polycrystalline structure with grains possibly in multiple orientations. In case of 20 V gate pulse, the retention time is around 15 minutes, which is three orders of magnitude longer than those of current generations

of conventional DRAMs. This is a substantial improvement and therefore quite attractive at least for the high speed direction of volatile memories.

### 5.1.4 Temperature Dependence

In general, the polarization changes with temperature. The derivative of the spontaneous polarization ($P_s$) over temperature can be written in Equation 5.2.

$$\frac{dP_S}{dT} = \gamma\,, \tag{5.3}$$

where γ is the pyroelectric coefficient that is not constant and depends on temperature [90], [91]. According to the suggestion of Ginzburg and Devonshire based on the phenomenological theory, the free energy of a ferroelectric material is given by Equation 5.3.

$$\Phi = \Phi_0 + \frac{1}{2}AP^2 + \frac{1}{2}BP^4 + \frac{1}{2}CP^6 + \cdots - EP, \tag{5.4}$$

where $\Phi_0$ is the free energy of the paraelectric phase [92], A, B and C are the development coefficients, E is the external electric field and P is the polarization. Coefficient A is a reciprocal of the electric susceptibility for the paraelectric phase (the Curie-Weiss law) and hence has a linear correlation with temperature as follows.

$$A = \alpha(T - T_c)\,, \tag{5.5}$$

where α is the proportional factor, T is the crystal temperature and $T_c$ is the Curie-Weiss temperature where the phase transition of a ferroelectric material occurs from the ferroelectric phase to the paraelectric one. Assuming the second-order phase

transitions, $P^6$ and higher order formula in Equation 5.3 can be ignored. While the electric field is zero and the derivative of Equation 5.3 is equal to zero, the free energy has a minimum value. Now, P becomes the spontaneous polarization ($P_s$) and its relation with temperature is as follows.

$$P_s^{\,2} = \frac{\alpha(T - T_c)}{\beta}, \tag{5.6}$$

where β is the coefficient B in the series of Equation 5.3. Therefore, assuming the second order phase transition, polarization has the square-root correlation with temperature near the Curie-Weiss temperature and hence one could extract the transition temperature from the extrapolation.

As shown in Figure 5.2 (b) and 5.9, the hysteresis window in response to the gate voltage does not disappear even at the temperature higher than the metal-insulator phase transition temperature (~70 ˚C). If the hysteresis is purely related to metal-insulator transition, the component should disappear above the transition temperature.

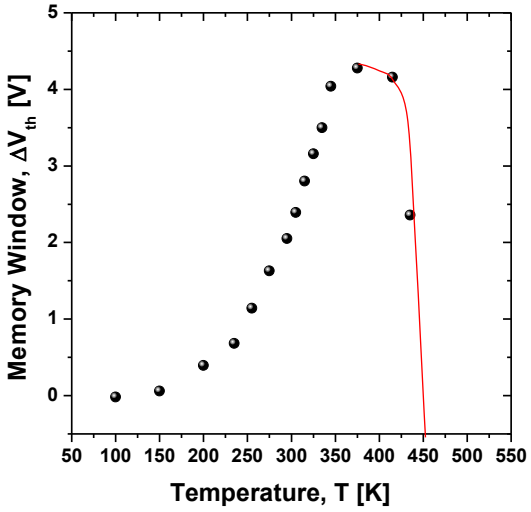



**Figure 5.9** Hysteretic memory window as a function of temperature.

The hysteresis, however, remains and the memory window increases all the more. This suggests the Curie-Weiss temperature of this ferroelectric transition for $VO_2$ is different from the metal-insulator transition temperature – probably significantly higher. That is, the ferroelectric mechanism of $VO_2$ may be independent of the metal-insulator phase transition mechanism. In Figure 5.9, memory window, which reflects the hysteresis window of the polarization, is defined as the difference in threshold voltage between forward and backward sweeps. As the temperature increases above 375 K, polarization decreases in the same way as other ferroelectric materials. Thus, using Equation 5.5, the Curie-Weiss temperature can be extracted and its value may be placed between 450 and 500 K. The other interesting observation is the degradation of the polarization of $VO_2$ at low temperatures. As the temperature decreased, the memory window reduced exponentially. For some ferroelectrics, below Curie temperature, this should not happen. But, there are ferroelectrics, such as strontium bismuth tantalate – $SrBi_2Ta_2O_9$ (SBT), where the freezing of switchable polarization has been observed [93]. The speculation is that domain pinning resulting from the deepening of the dual valley phase transition potential well causes this. In SBT, 180° domain walls dominate and the wall potential is argued to have a box-like shape and deepen at low temperature [94], in turn inducing defects that pin the domain [93]. That is, with decreasing temperature, the amount of switchable polarization reduces due to the domain pinning. We speculate that the mechanism of polarization freezing in $VO_2$ is the same as that of SBT.

## *5.2 GST Devices*

### 5.2.1 Phase transition by external heating and cooling

Figure 3.10 and 5.10 show the resistance change of GST after external heating and cooling. First, the resistance change was measured in hall bar test pattern which doesn't have transistor process, meaning that the GST film keeps initial status as it was sputtered. The resistance is about 500 kΩ, which is close to the value of GST in the amorphous phase [95]. In contrast, when all transistor-making processes are employed, the resistance is around 7 kΩ, which is close to the value of GST in the metastable FCC crystalline phase. So, the fabrication processes can make an effect on the initial phase of GST. To prevent GST from changing its phase from amorphous to FCC crystalline during fabrication processes, it is necessary to control all the processes under 150 ℃ of the phase change temperature. After $H_2$ anneal at 300 ℃ in

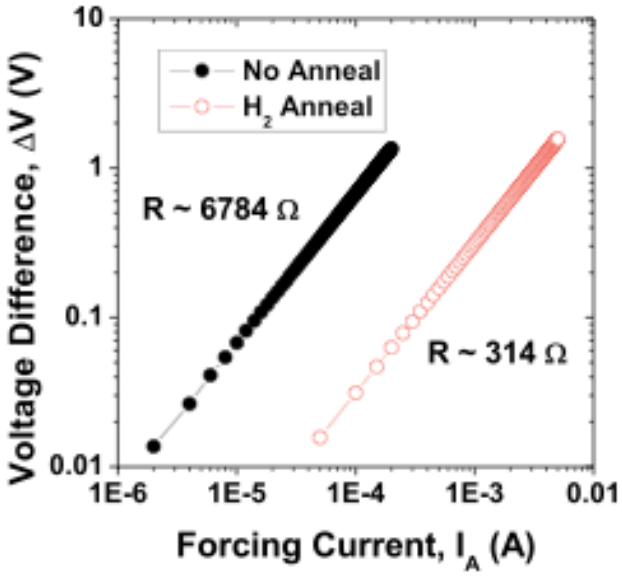



**Figure 5.10** GST resistance change before and after $H_2$ annealing at 300 ℃ in flowing 5 % $H_2$ for 1 hr.

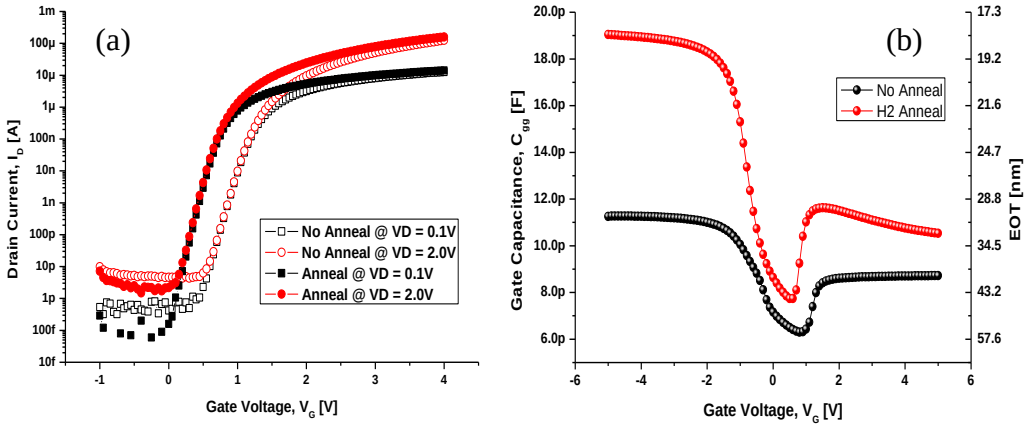



**Figure 5.11** $H_2$ annealing effect: (a) Threshold voltage shift and (b) capacitance change before and after $H_2$ annealing at 300 ℃ in flowing 5 % $H_2$ for 1 hr.

flowing 5 % $H_2$ for 1 hr, the resistance decreases to about 300 Ω being close to the value of GST in the HCP crystalline phase. Once the phase of GST becomes HCP crystalline, thermal hysteresis behavior disappears and GST acts like a metal. In this phase, when the temperature increases, the resistance also increases due to the increase of phonon scattering.

Before measuring the effect of joule heating, the threshold shift and capacitance change was investigated with the external heating. As shown in Figure 5.11, after $H_2$ anneal, the threshold voltage decreases and gate capacitance increases. $\Delta V_{th}$ and $\Delta C_{acc}$ are 0.5 V and 8 pF, respectively. It shows that the dielectric constant of GST changes due to its phase transition. Unlike the results of external heating, the effect of joule heating is small and relatively not reproducible as shown in Figure 5.12. After DC stress in various conditions, the threshold voltage changes slightly. Compared to high $V_{DS}$ condition, the $V_{th}$ shift is, however, larger in low $V_{DS}$ condition. It tells that some change is likely to happen at the drain edge mainly as expected from

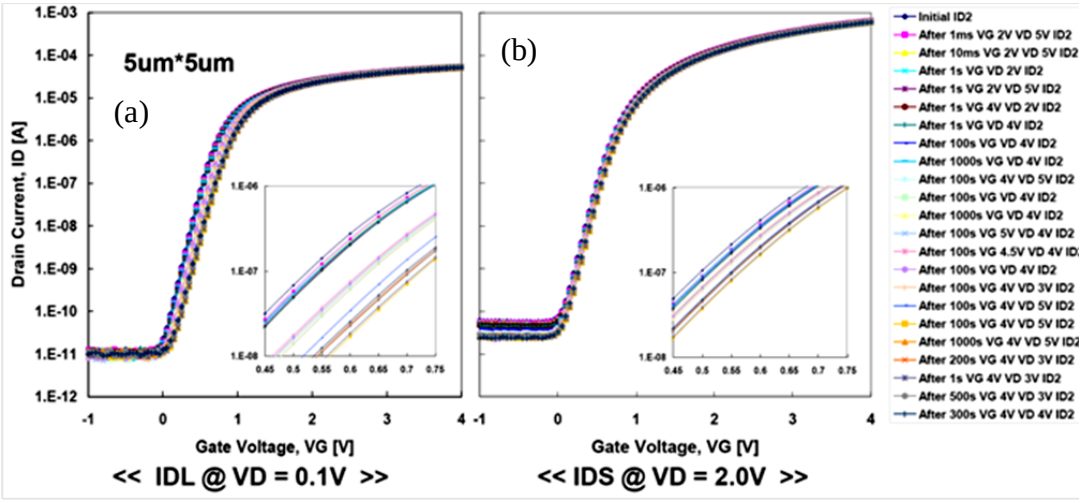



**Figure 5.12** Threshold voltage changes with DC stress in various bias conditions: (a) Linear threshold voltage and (b) saturated one.

the thermal simulation. The main reason for this little change is that the heat generated in the channel can dissipate through the substrate more easily than be delivered to a phase transition material through the gate oxide because the thermal conductivity of silicon is about 150 times higher than that of silicon dioxide. Therefore, unlike the simulation results of a SOI transistor, the temperature of the channel and the heat transfer efficiency must be lower than expected. The heating efficiency can be improved by use of silicon-on-insulator (SOI), wire and other forms where heat transport through the substrate is suppressed.

Additionally, the possibility of gate field induced phase transition using modified HB test patterns in Figure 4.5 (b) was examined. If the phase of GST is controlled by the gate field, one can enlarge the memory window and acquire another option to manipulate data. Figure 5.13 shows the resistance change in response to the gate field. In the positive field, the resistance increases as the field intensity increases.

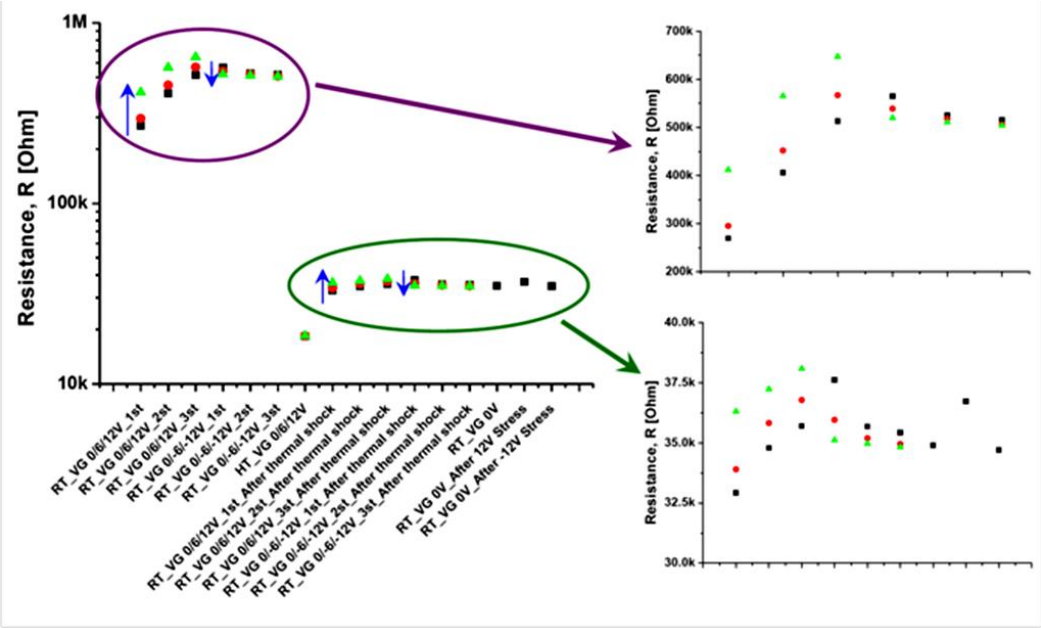



**Figure 5.13** Resistance change in response to the gate field.

On the other hand, in the negative field, the resistance decreases as the field intensity increases. In the amorphous phase, the resistance variation is larger than in the FCC crystalline, but the trend of field dependency is the same in both phases. This is the very first discovery implying that the gate field can affect the phase transition mechanism of GST.

### 5.2.2 Ferroelectric properties

Like $VO_2$ devices, GST devices have hysteretic behaviors in response to the gate voltage. As discussed in Chapter 3, in the FCC crystalline phase of GST, Ge atoms shift from the ideal rocksalt positions. These off-centered displacements result in a net dipole moment. This suggests that FCC GST is a ferroelectric material. As shown in Figure 5.14 (a), the hysteresis window is smaller than that of a $VO_2$ device. However, the cycling direction of the hysteresis is counterclockwise like $VO_2$ devices.

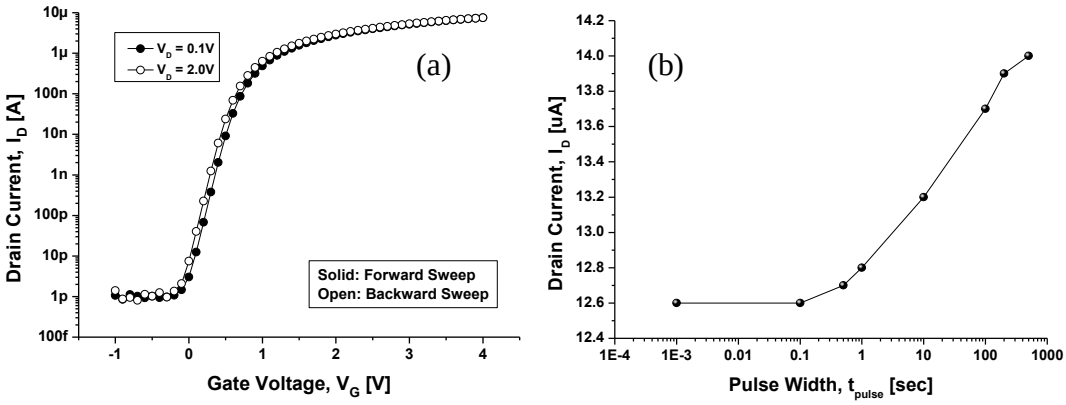



**Figure 5.14** Ferroelectric properties of GST: (a) Counterclockwise current-voltage hysteresis and (b) data writing characteristics with 2V gate voltage. After the gate pulse, the drain current was measured at $V_{GS}$ = 2 V and $V_{DS}$ = 2 V.

In addition, data writing time is similar to that of a $VO_2$ device as shown in Figure 5.14 (b). When the gate pulse amplitude is 3 V, the required writing time is above 0.1 msec. These results imply that the hysteretic behaviors of GST devices are also caused by the ferroelectric polarization of GST, not by the heat-triggered phase transition of GST.

## *5.3 SNO Devices*

### 5.3.1 Dielectric Properties and Hysteretic behaviors

Using a MOS capacitor structure, the dielectric properties of a SNO thin film were characterized and analyzed. Figure 5.15 shows the capacitance-voltage (C–V) characteristics of a MOS capacitor in response to gate voltage at various temperatures. The dielectric constant of SNO can be extracted from the structural parameters and capacitance. It is around 26 at room temperature and so equivalent oxide thickness (EOT) is ~100 nm. The extracted dielectric constant is in good agreement with optical

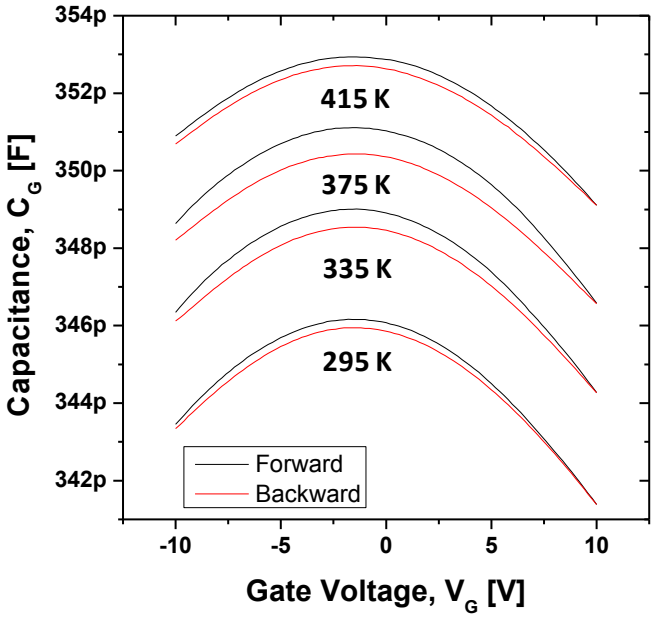



**Figure 5.15** Voltage hysteresis and temperature dependence of the gate capacitance of a MOS capacitor with an n+ silicon substrate.

measurements of the closely related material $NdNiO_3$ [96]. As shown in the figure, the voltage hysteretic behavior of capacitance is observed. Capacitance during a forward sweep increases initially and has a peak value at a certain gate voltage, around -1.6 V and then decreases. During a backward sweep, similar effect happens, but its magnitude is lower compared to the forward measurement. Note that the asymmetry of C–V curves is caused by the work function difference of the metal electrodes and internal built-in electric field [97]. Similar hysteretic behavior was also observed in a $SrTiO_3$ (STO) film. Buniatian et al. explained that the hysteresis effects are caused by excess space charge, such as oxygen vacancies, and proposed a model based on the Poole-Frenkel charge trapping/detrapping mechanism [98]. According to their model, oxygen vacancies are potential sites for this space charge effect, and deformation of the dipole distribution and change in the permittivity of the STO film are subject to

charge trapping/detrapping of the oxygen vacancies. Without external electric field, the oxygen vacancies are assumed to be neutral due to trapped electrons. Under an applied electric field, the electrons are detrapped and hence the vacancies are positively charged. The internal electric field generated by the charged vacancies changes the polarization of the surrounding crystal locally and hence reduces its permittivity. As mentioned before, the SNO film also has oxygen vacancies and its hysteretic behavior is likely induced by space charge polarization of oxygen vacancies.

Figure 5.16 shows the results of peak capacitance variation as a function of the applied ac signal frequency. As shown in figures, the capacitance and its voltage hysteresis window increase as the frequency decreases. This implies that the dielectric polarization of SNO changes with the frequency. The permittivity of a dielectric material depends on the frequency of the applied field since there are various polarization mechanisms and each type of polarization has a different response time. For example, space charge polarization has a relaxation frequency of around 100 kHz. In case of SNO, the dielectric constant changes with the frequencies ranging between 20 Hz and 1 MHz, which means that the response time of polarization is above 1 μs. Therefore, space charge polarization is dominant in the permittivity of the SNO film.

### 5.3.2 Memory effects in MOSFET devices

As expected from the results of a MOS capacitor, hysteretic behavior of gate capacitance between gate and S/D in response to gate voltage is observed with similar frequency dependence as shown in Figure 5.17. As the gate voltage is cycled between–10 and 10 V, the capacitance cycles counterclockwise. This hysteretic

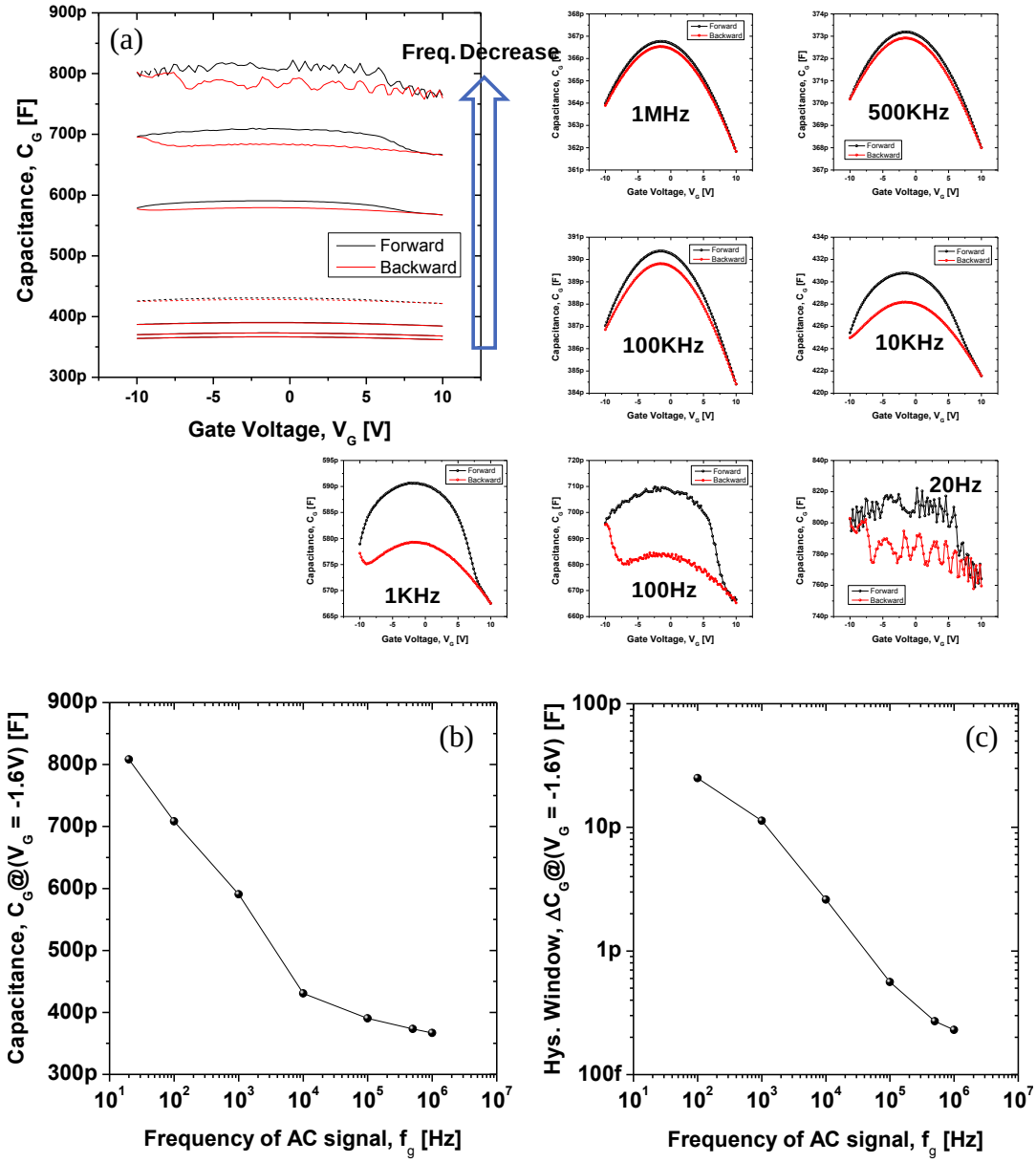



**Figure 5.16** MOS capacitance change with the frequency of ac-signal: (a) Capacitance-voltage plots with various frequencies and frequency dependence of (b) the gate capacitance and (c) the hysteresis window with a n+ silicon substrate.

behavior is opposite of the hysteresis resulting from charge trapping in the gate insulators and is consistent with polarization switching. Similar hysteretic effect occurs in current-voltage (IV) characteristics of a transistor. Since the threshold voltage shift happens even in the absence of channel current, it is a gate field effect. In

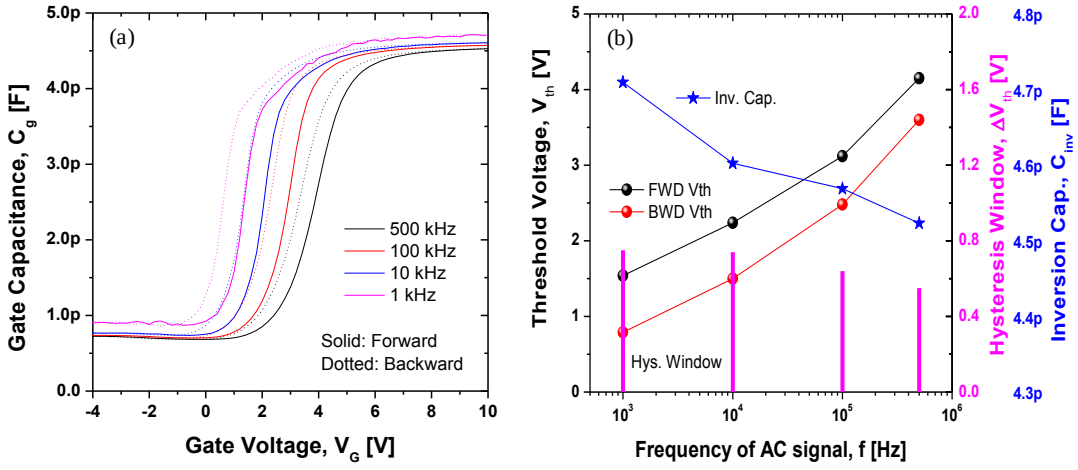



**Figure 5.17** Frequency dependence of the gate capacitance of a MOSFET device: (a) C–V curves with various frequency and (b) threshold voltage, hysteresis window and inversion capacitance vs. frequency correlation plots.

addition, it occurs at room temperature. Therefore, this effect is independent of the thermally-driven metal-insulator phase transition of SNO. With the decrease of frequency, threshold voltage decreases substantially, and hysteresis window and inversion capacitance increase slightly. This implies that polarization change makes an effect on the change of threshold voltage dominantly. These results, their existence with a gate field, their existence in the absence of heating, and frequency dependence, can be explained through space charge polarization mechanism in the SNO film. Figure 5.18 shows the temperature dependence of the voltage hysteresis of gate capacitance. As temperature increases, threshold voltage decreases and inversion capacitance increases. Hysteresis window is the most changeable factor and has a peak at around 385 K which is close to metal-insulator phase transition temperature. The hopping polarizability ( $\alpha_h$) induced by oxygen vacancies is correlated with temperature as follows [19].

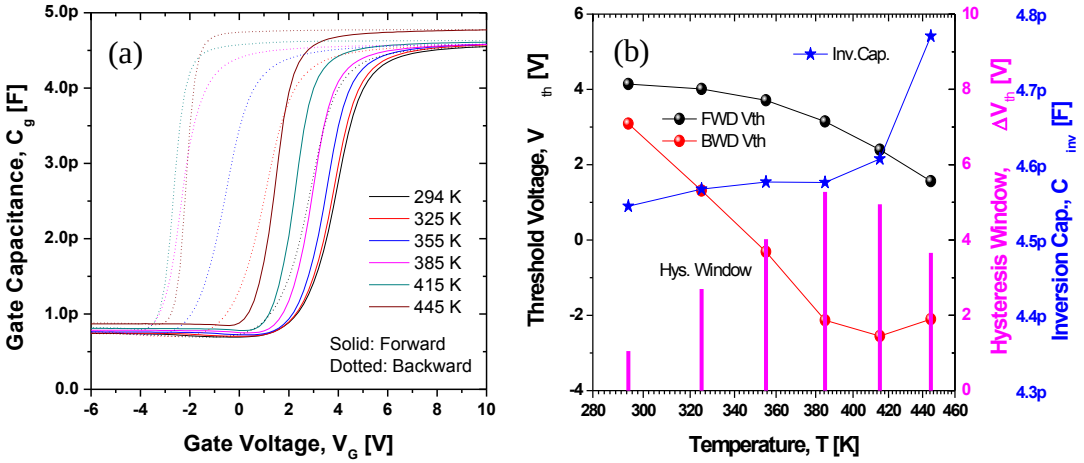



**Figure 5.18** Temperature dependence of the gate capacitance of a MOSFET device: (a) C–V curves with various temperature and (b) threshold voltage, hysteresis window and inversion capacitance vs. temperature correlation plots.

$$\alpha_h{}^2 = \frac{q^2 r^2}{3kT} \overline{P_{0(A\to B)} P_{0(B\to A)}}\,, \tag{5.7}$$

where r is the distance between two peaks of a double potential, $P_{0(A\to B)}$ is the time-averaged probability for a charged particle to hop from site A to site B without an applied electric field, $P_{0(B\to A)}$ is the probability for the charged particle to hop in the reverse direction, and $\overline{P_{0(A\to B)} P_{0(B\to A)}}$ denotes the ensemble average of the product of these two probabilities. The probabilities are

$$P_{0(A\to B)} = Cexp(-\frac{E_A}{kT})\,, \tag{5.8}$$

$$P_{0(B\to A)} = Cexp(-\frac{E_B}{kT})\,, \tag{5.9}$$

where C a constant, $E_A$ is the activation energies for the hopping transition from site A to site B, and $E_B$ is the activation energy from site B to site A. According to Equation

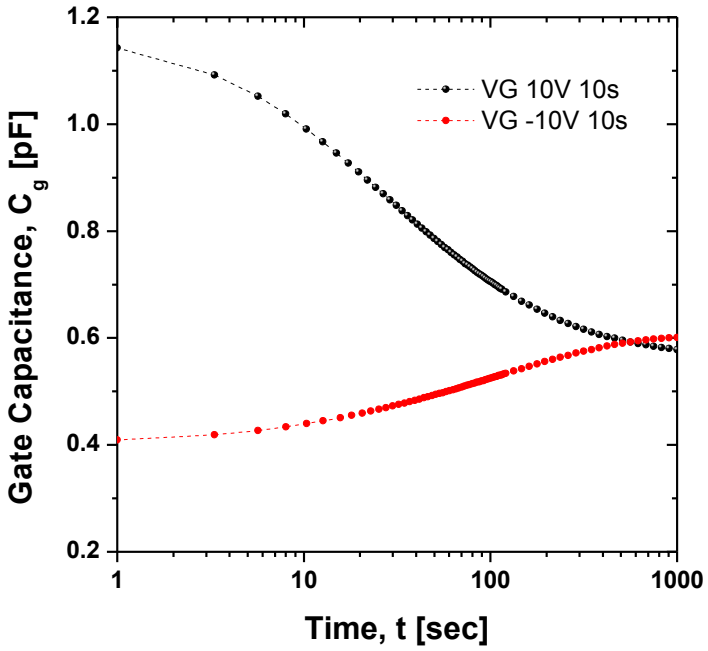



**Figure 5.19** State retention characteristics of a MOSFET device. The gate capacitance at zero gate bias is measured after applying a gate pulse.

5.6, the polarization has a maximum value at a certain temperature, which corresponds with the correlation of the hysteresis window with temperature. However, more study is needed to figure out the exact physical mechanism of this effect. The sharp increase in inversion capacitance may be related to the MIT effect. Unlike the frequency dependence, polarization change seems to affect both threshold voltage and hysteresis window.

To measure the state retention characteristics of SNO devices, the gate capacitance at zero gate bias is measured after applying a gate pulse to suppress data interference during the measurement. As shown in Figure 5.19, the state decays gradually. It is believed that the depolarization field generated internally due to the finite dielectric constant of silicon substrate, unlike that of a metal, degrades the polarization of a SNO film. The state retention time is of the order of ten seconds.

## 5.4 Summary

The results of bulk-type phase transition memory transistors have been discussed. Irrespective of phase transition materials, hysteretic behaviors are present in all devices in response to the gate voltage at room temperature. The cycling directions of hysteresis are counterclockwise, which indicates that this effect results from the polarization switching of the phase transition materials considering that the gate oxides are thick enough to suppress charge injection into the gate insulators. With only a gate field, the threshold voltage is modulated at room temperature. Therefore, this is a gate field effect, not a thermally-driven phase transition effect. In case of $VO_2$ and GST, their hysteretic behaviors are caused by the ferroelectric polarizations given the fact that $VO_2$ has an off-centered vanadium ions and GST has the displacement of Ge ions in their crystal structures resulting in net dipole moments. According to the temperature dependence of hysteresis memory window of $VO_2$ devices, the Curie-Weiss temperature of $VO_2$ is different from the metal-insulator phase transition temperature. That is, the ferroelectric mechanism of $VO_2$ may be independent of the metal-insulator phase transition mechanism. Assuming the second order phase transition, polarization has the square-root correlation with temperature near the Curie-Weiss temperature. From the extrapolation, the Curie-Weiss temperature of $VO_2$ is extracted and its value is around 450 K. At lower temperatures, the polarization of $VO_2$ disappears exponentially. It is believed that the origin for the low temperature effect of polarization may arise from the freezing of switchable polarization. SNO has non-negligible oxygen vacancies due to the instability of the $Ni^{3+}$ valence state and hence space charge polarization is dominant. Due to the intrinsic depolarization field

and charge injection, the presented devices are volatile with the state retention times of the order of minutes.

# Chapter 6

# CHARACTERIZATION OF SUSPENDED CHANNEL DEVICES

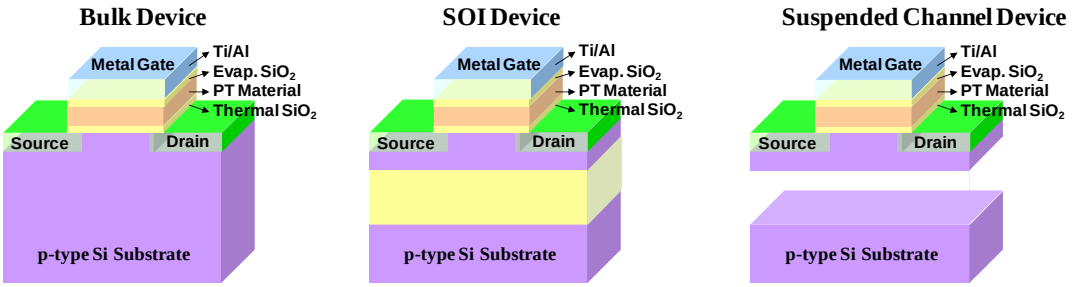
This chapter discusses the heat transfer efficiencies of several device structures: bulk-type, SOI and suspended channel devices. To calculate the heat transfer efficiency, two simple models are presented: pyramidal and radial heat conduction models. The suspended channel device with an air-gap under the channel has the best efficiency of around 85%. The suspended channel structure is implemented in GST devices. However, ferroelectric effect dominates over the phase transition property of GST.

## *6.1 Heat Transfer Efficiency Improvement*

Heat transfer efficiency is defined by the ratio of heat energy delivered to the gate stack to the total dissipated one as shown in Equation 2.6. According to the law of heat conduction, also known as Fourier's law, heat flow rate (H) through a material is proportional to the gradient of temperature ($^{\Delta T}/_{\Delta L}$) and the area (A) like this equation.

$$H = \frac{\Delta Q}{\Delta t} = kA\frac{\Delta T}{\Delta L} = G\Delta T = \frac{\Delta T}{R}\ \left(R = \frac{1}{G} = \frac{\Delta L}{kA}\right), \tag{6.1}$$

The proportional constant in the equation is the thermal conductivity (k) of a material and thermal resistance (R) is the reciprocal thermal conductance (G). Therefore, if one




$R_{down} = R_{sub}$
$\alpha \sim 1.9\%$ @$VO_2$
$\alpha \sim 1.2\%$ @GST

$R_{down} = R_{Si} + R_{SOI} + R_{sub}$
$\alpha \sim 17\%$ @$VO_2$
$\alpha \sim 11\%$ @GST

$R_{down} = R_{Si} + R_{Air} + R_{sub}$
$\alpha \sim 88\%$ @$VO_2$
$\alpha \sim 82\%$ @GST

- $\alpha * I_{ch}^2 * R_{ch} * t_{sw}$ (Joule Heating Energy) = $m_{ox} * c_{ox} * \Delta T$ (Oxide Heating Energy) + $L_{PT} * V_{PT}$(Latent Heat of Phase Transition Material)
- $\alpha$ (Heat Efficiency) = $H_{up} / (H_{up} + H_{down}) = R_{down} / (R_{up} + R_{down})$
- $H = \Delta Q/\Delta t = k*A/L*\Delta T = \Delta T/R$ ; k ≡ thermal conductivity, R ≡ thermal resistance
- $R_{up} = R_{BO} + R_{PT} + R_{TO} + R_{Ti} + R_{Al}$
- $k_{Ox} = 1$, $k_{Si} = 149$, $k_{Air} = 0.025$, $k_{VO2} = 3.5$, $k_{GST} = 1.2$, $k_{Ti} = 22$, $k_{Al} = 237$ [W/mK]
- $T_{BO} = 10$, $T_{PT} = 50$, $T_{TO} = 20$, $T_{Ti} = 50$, $T_{Al} = 300$, $T_{Si} = 340$, $T_{SOI} = 400$, $T_{sub} = 5*10^5$ [nm]
- Channel Length & Width = 100 [nm]

**Figure 6.1** Schematics and heat transfer efficiencies of several device structures: bulk-type, SOI and suspended channel devices. The efficiency in the figure is calculated using the pyramidal heat conduction model.

knows the resistance and the temperature difference between the ends, heat flow rate can be acquired.

Figure 6.1 shows the structures of several phase transition devices proposed to improve the heat transfer efficiency. To maximize the heat transfer to phase transition materials, one needs to increase the thermal resistance below the channel. Thus, SOI devices with an oxide layer under the channel and suspended channel devices with an air-gap under the channel are proposed. The thermal conductivities of silicon dioxide and air are 150 times and 6000 times lower than that of silicon, respectively. Therefore, the new high thermal impedance structures with silicon dioxide or air-gap should have efficient heat delivery to the phase transition material.

Joule heat generated by channel current transfers through the layers to the ends. It goes through the gate insulator layers upwardly and through the substrate downwardly. Thus, each directional resistance can be acquired by the below equations.

$$R_{up} = R_{BO} + R_{PT} + R_{TO} + R_{Ti} + R_{Al}\,, \tag{6.2}$$

$$R_{down} = R_{sub}\ for\ a\ bulk - type\ device\,,$$

$$= R_{Si} + R_{SOI} + R_{sub}\ for\ a\ SOI\ device\,,$$

$$= R_{Si} + R_{Air} + R_{sub}\ for\ a\ suspended\ channel\ device\,, \tag{6.3}$$

where $R_{BO}$, $R_{PT}$, $R_{TO}$, $R_{Ti}$, $R_{Al}$, $R_{sub}$, $R_{Si}$, $R_{SOI}$ and $R_{air}$ are the thermal resistances of bottom gate oxide, phase transition material, top gate oxide, titanium metal layer, aluminum metal layer, Si substrate, buried oxide layer of SOI wafer and air-gap of the suspended channel device, respectively. When thermal resistances connect in series, total resistance is equal to the sum of resistances. So, the resistance is calculated by integration of small pieces of resistances in series like this equation.

$$R = \int_0^R dR = \int_0^L \frac{dx}{kA(x)}\,, \tag{6.4}$$

Here, a model to define a cross-sectional surface as a function of x is needed. As shown in Figure 6.2, in this thesis, two simple models are presented: pyramidal heat conduction model and radial heat conduction model. In the pyramidal heat conduction model, the each side of the cross-sectional surface, which should be square, is

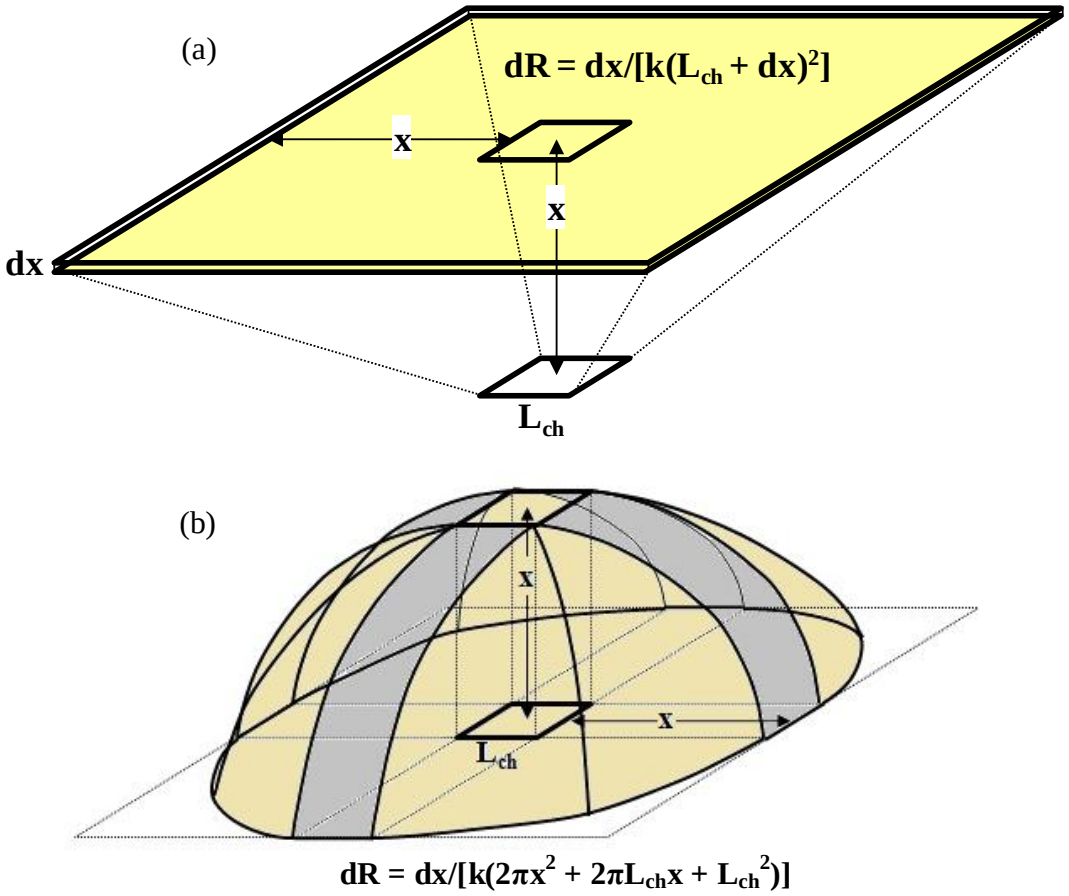



**Figure 6.2** Simple models for the calculation of thermal resistance: (a) Pyramidal heat conduction model and (b) radial heat conduction model.

assumed to increase by the distance between the channel and the surface. So, the area of the cross-sectional surface is equal to

$$A(x) = (L_{ch} + 2x)^2 \,, \tag{6.5}$$

where $L_{ch}$ is the length of the channel and x is the distance between the channel and the surface. Substituting Equation 6.5 into equation 6.4, the thermal resistance of each layer can be acquired with the below integration.

$$R = \int_{L_1}^{L_2} \frac{dx}{kA(x)} = \frac{1}{k}\int_{L_1}^{L_2} \frac{1}{(L_{ch}+2x)^2}\,dx = \frac{1}{2k}\left[-\frac{1}{L_{ch}+2x}\right]_{L_1}^{L_2}. \quad (6.6)$$

In the radial heat conduction model, every point of the cross-section surface is assumed to increase radially by x. So, the surface is composed of three elements: a square with the area of $L_{ch}{}^2$, a cylinder with the area of $2\pi L_{ch}x$ and a half sphere with the area of $2\pi x^2$.

$$A(x) = 2\pi x^2 + 2\pi L_{ch}x + L_{ch}{}^2. \quad (6.7)$$

Substituting Equation 6.7 into equation 6.4, the thermal resistance of each layer can be acquired with the below integration.

$$R = \int_{L_1}^{L_2} \frac{dx}{kA(x)} = \frac{1}{k}\int_{L_1}^{L_2} \frac{1}{2\pi x^2+2\pi L_{ch}x+L_{ch}{}^2}\,dx$$

$$= \frac{1}{k\mathcal{L}}\left[log(4\pi x - \mathcal{L} + 2\pi L_{ch}) - log\ (4\pi x + \mathcal{L} + 2\pi L_{ch})\right]_{L_1}^{L_2}, \quad (6.8)$$

$$(\mathcal{L} \equiv 2\sqrt{\pi}\sqrt{\pi - 2}L_{ch})$$

Table 6.1 shows the results of the thermal resistances and heat transfer efficiencies from the calculations from the above cross-sectional surface models. A GST device has lower efficiency than a $VO_2$ device because the thermal conductivity of GST is lower than that of $VO_2$. The radial model gives lower efficiency than the pyramidal model. This is caused by the difference of the surface area between two models. The surface area calculated from the radial model is bigger than that from the pyramidal model. As a result, the thermal resistance of the radial model is lower than

**Table 6.1** Thermal resistances and heat transfer efficiencies calculated from the proposed cross-section surface models.

| | | Pyramidal Model | | | Radial Model | | |
|---|---|---|---|---|---|---|---|
| | | $VO_2$ / GST | | | $VO_2$ / GST | | |
| | | Bulk | SOI | Airgap | Bulk | SOI | Airgap |
| $R_{up}$ [$m^2K/W$] | $R_{BO}$ | 8.33E+05 | | | 7.66E+05 | | |
| | $R_{PT}$ | 5.41E+05 / 1.58E+06 | | | 4.09E+06 / 1.19E+06 | | |
| | $R_{TO}$ | 3.50E+05 | | | 2.38E+05 | | |
| | $R_{Ti}$ | 2.43E+04 | | | 1.61E+04 | | |
| | $R_{Al}$ | 3.66E+03 | | | 2.37E+03 | | |
| | Total | 1.75E+06 / 2.79E+06 | | | 1.43E+06 / 2.22E+06 | | |
| Rdown [$m^2K/W$] | $R_{Si}$ | | 2.93E+04 | | | 2.20E+04 | |
| | $R_{SOI}$ | | 3.25E+05 | | | 2.07E+05 | |
| | $R_{Air}$ | | | 1.30E+07 | | | 8.29E+06 |
| | $R_{sub}$ | 3.36E+04 | 2.12E+03 | | 2.47E+04 | 1.35E+03 | |
| | Total | 3.36E+04 | 3.56E+05 | 1.30E+07 | 2.47E+04 | 2.31E+05 | 8.32E+06 |
| Heat Transfer Efficiency [%] | | 1.9 / 1.2 | 16.9 / 11.3 | 88.1 / 82.4 | 1.7 / 1.1 | 13.9 / 9.4 | 85.3 / 79.0 |

that of the pyramidal model. The heat transfer efficiencies are 1.1 ~ 1.9% for the bulk-type device, 9.4 ~ 16.9% for the SOI device and 79.0 ~ 88.1% for the suspended channel device.

## *6.2 GST Devices*

### 6.2.1 Ferroelectric properties

Compared to the results of GST bulk-type devices, the hysteresis windows of GST suspended channel devices increase, which are comparable to those of $VO_2$ bulk devices. In spite of the improvement of the heat transfer efficiency with the implementation of a suspended channel structure, heat triggered phase transition effect

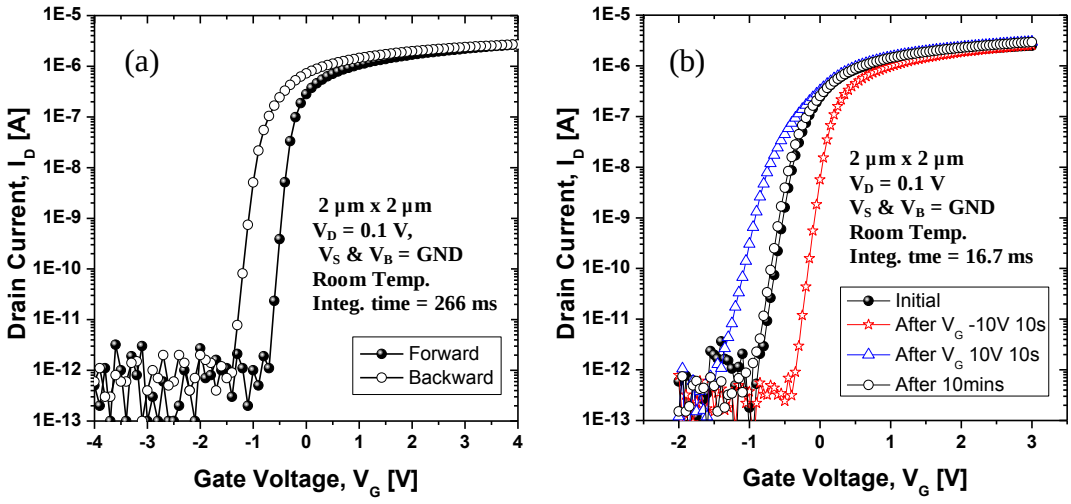



**Figure 6.3** Threshold voltage shift due to ferroelectric polarization switching: (a) Hysteresis behavior of drain current in response to gate voltage. (b) Gate field dependence of threshold voltage shift.

has not been observed. Figure 6.3 (a) shows the hysteresis behavior of drain current at room temperature in response to the gate voltage. For the gate voltage cycling between -4 and 4 V (starting from -4 V), the drain current cycles counterclockwise. The memory window is ~1 V, which is almost the same value as that of a $VO_2$ bulk device. Figure 6.3 (b) shows the threshold voltage shift after gate pulsing. Similar hysteretic effect occurs in capacitance measurement where no channel current flows. This hysteresis behavior is consistent with ferroelectric polarization switching and opposite of the hysteresis resulting from channel electron charge trapping in the gate insulators [99]. Note also that the insulator thicknesses are very large and the fields under biases very small. So, it is expected that low voltage operation can be realized when the thicknesses of gate insulators are reduced. After applying the negative gate voltage, the threshold voltage shifts positively and vice versa and since the shift happens even in the absence of channel current, it is a room temperature effect and a field effect. It is

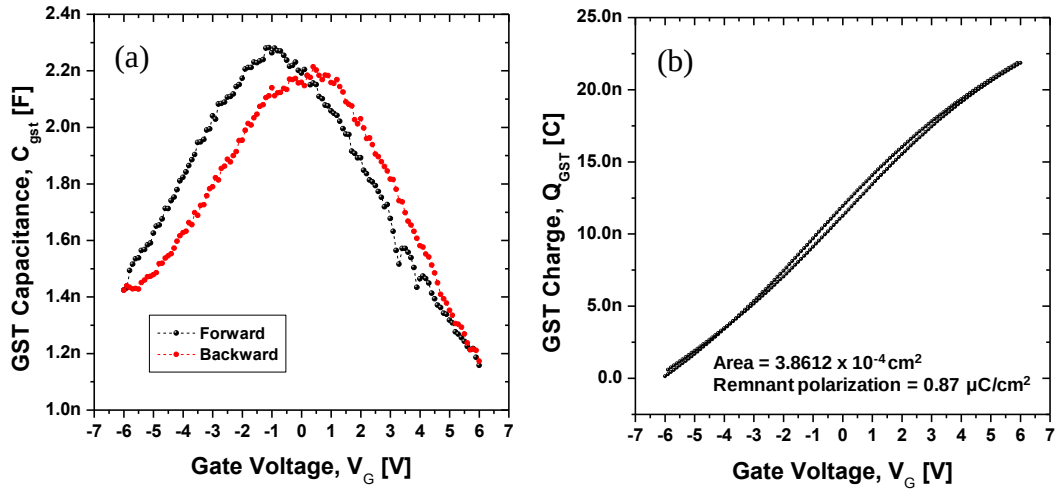



**Figure 6.4** Typical ferroelectric curves: (a) Butterfly curve of the capacitance and (b) polarization charge hysteresis curve in response to the gate voltage.

not due to structural phase transition that is commonly employed, not due to heating and not due to charge injection. The measured windows reduce with time. For example, after 10 min., the threshold voltage nearly returns to the initial value as shown in Fig. 6.3 (b). This recovery implies that similar to other ferroelectric memories, depolarization field is generated in the GST film. In short, these results are consistent with the postulation of ferroelectric polarization mechanism in the GST film.

Furthermore, a butterfly curve of the capacitance with the gate electric field, which is believed to be typical for ferroelectrics, is observed in a large area capacitor as shown in Figure 6.4 (a). The polarization charge hysteresis curve in response to the gate voltage is shown in Figure 6.4 (b). The remnant polarization is ~0.87 μC/cm$^2$. The remnant polarization can be also extracted from the saturation characteristics of the threshold voltage shift of a MOSFET device. As shown in Figure 6.5, the threshold voltage shift saturates as the sweeping range of the gate bias reaches at ~10 V. This

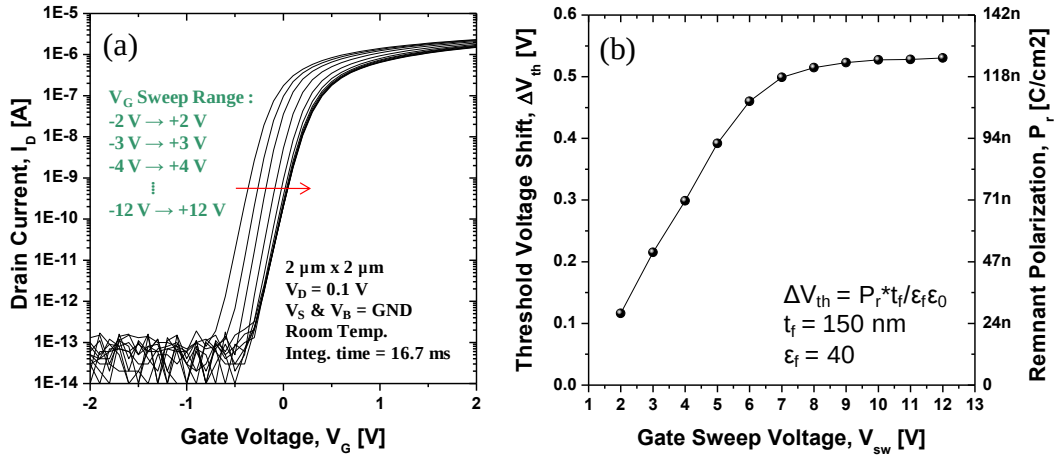



**Figure 6.5** Saturation in threshold voltage shift as gate sweeping voltage increases: (a) VG-ID curves at various gate sweeping voltages and (b) threshold voltage shift as a function of gate sweep voltage.

implies that the polarization of GST saturates at 10 V and GST film has the remnant polarization when the gate field is removed. The extracted remnant polarization of GST from the threshold voltage shift and structural parameters is ~0.13 µC/cm$^2$. This value is comparable to the minimum polarization for a FeDRAM. However, the additional experiments are needed to figure out why the remnant polarization extracted from a MOSFET structure with a small area is much smaller than the value extracted from a large area capacitor.

### 6.2.2 Data writing and retention characteristics

Like other ferroelectric memory devices, the polarization of a GST device decays gradually due to the depolarization field. As discussed in Chapter 5, the depolarization field is fundamental to a ferroelectric memory with a semiconductor substrate because of the finite dielectric constant of the semiconductor. Figure 6.6

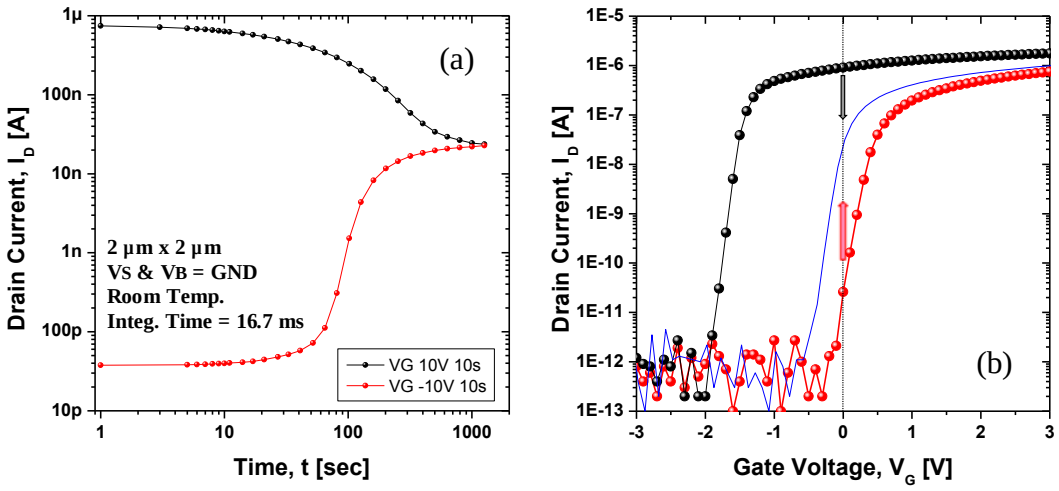



**Figure 6.6** State Retention characteristics of a GST floating gate device: (a) Drain current as a function of time and (b) the threshold voltage change with time. Drain current is measured when the gate and drain voltage are 0 V and 50 mV after applying the gate pulse.

shows the state retention characteristics of a GST device. To measure the state retention time, the off-state drain current is sampled when the gate and drain voltage are 0 V and 50 mV, i.e., under near-short-circuit conditions, after applying a gate pulse. The device has strong gate field dependence. One therefore needs a near-short-circuit condition to suppress measurement artifact on the device state. Off-state drain current has a strong correlation with threshold voltage when it is determined by the sub-threshold properties. So, Off-state current here reflects the change of threshold voltage induced by the polarization degradation. The retention time is around 100 seconds at room temperature. This is longer than of DRAMs by about two orders of magnitude and thus a substantial improvement over the current generation of conventional DRAMs.

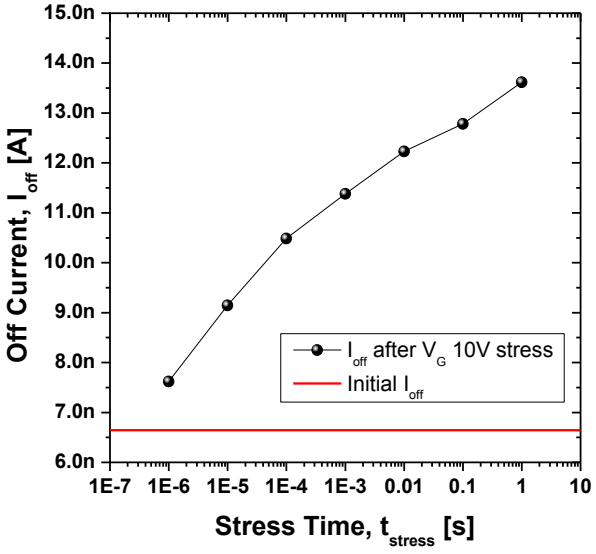



**Figure 6.7** Data writing characteristics: Increment of the Off-state current as a function of gate pulse width is observed.

Figure 6.7 shows the data writing time of GST devices. To measure the writing time, the increment of the Off-state current as a function of gate pulse width is observed. As shown in the figure, data writing time is faster compared to bulk-type devices (~0.1 ms). Even when the pulse width of the gate voltage is 1 μs, the Off-state current increases due to threshold voltage shift. However, this value is still higher than those of other dynamic memories. Given the fact that the ferroelectric switching takes place in below nanoseconds, the devices themselves are expected to be much faster.

### 6.2.3 Temperature dependence

Like the $VO_2$ bulk-type device, the disappearance of the polarization reflected by the change of hysteresis memory window is observed at low temperatures. Memory window is defined as the difference in threshold voltage between forward and

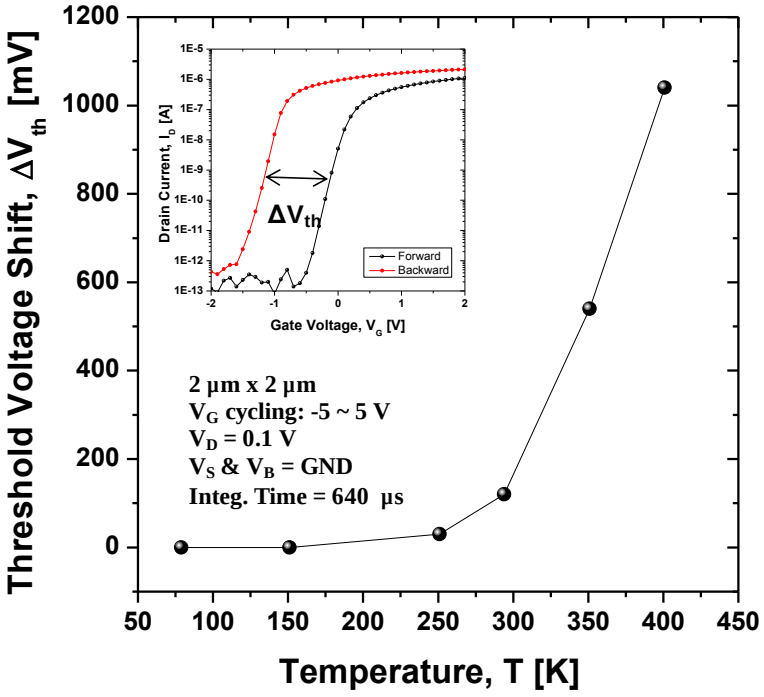



**Figure 6.8** Temperature dependence of the hysteresis memory window. The polarization of GST is reflected in the threshold voltage shift. Inset in this figure shows the threshold voltage shift at 400 K.

backward sweeps. Figure 6.8 shows the temperature dependence of the hysteresis memory window – a reduction as temperature is lowered. As discussed in Chapter 5, SBT has the same temperature effect. Yang et al. argued that this effect results from the freezing of switchable polarization due to domain pinning induced by the deepening of the dual valley phase transition potential well [93]. For now, we speculate that the mechanism of polarization freezing in GST is the same as that of SBT and need more study on this phenomenon to confirm the speculation. Figure 6.9 shows another interesting observation at low temperature. Contrary to the hysteresis of the drain current at high temperature, the clockwise cycling hysteresis is observed at 79 K. This effect is consistent with the hysteresis induced by charge trapping in the

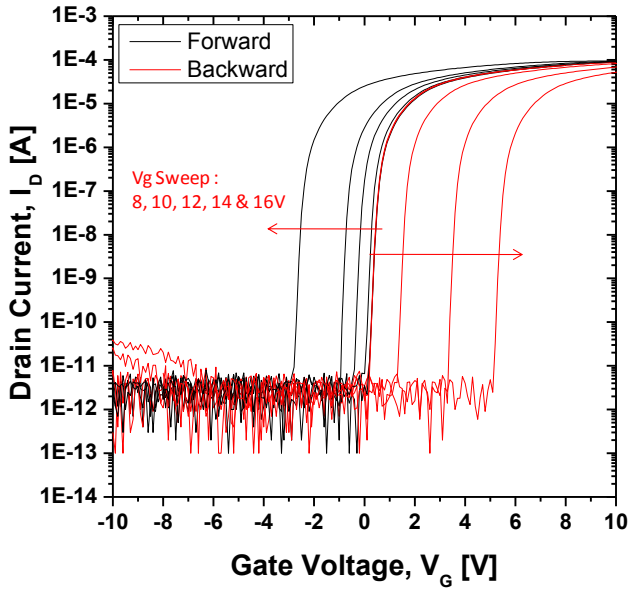



**Figure 6.9** Clockwise hysteresis of the drain current at 79 K. This effect is consistent with the hysteresis induced by charge trapping in the gate insulators.

gate insulators. This is likely to be related to the degradation of polarization at low temperature, because the cycling direction of the hysteresis is opposite and hence this can offset the hysteresis memory window induced by the ferroelectric polarization. In addition, charge trapping induced by tunneling current has a weak dependence on temperature and even at low temperature, charge trapping effect still remains. That is, at high temperature, ferroelectric polarization effect dominates over other effects, but disappears exponentially with the decrease of temperature due to the freezing of switchable polarization. Then, charge trapping effect can be observed at low temperature.

## 6.3 Summary

The heat transfer efficiencies of several device structures have been discussed. To acquire the areas of cross-sectional surfaces for the integration of thermal resistance, pyramidal and radial heat conduction models were established and the heat transfer efficiency is 1.1 ~ 1.9% for the bulk-type device, 9.4 ~ 16.9% for the SOI device and 79 ~ 88.1% for the suspended channel device. A GST device has lower efficiency than a $VO_2$ device and the radial model gives lower efficiency than the pyramidal model. The suspended channel structure was implemented in GST devices. However, ferroelectric effect dominated over the phase transition property of GST. The extracted remnant polarization of GST is ~0.13 μC/cm2. The retention time is the order of hundred seconds and the writing time is the order of microseconds. The degradation of the polarization is observed at low temperature and this seems to result from the freezing of switchable polarization and charge trapping in the gate insulator.

# Chapter 7

# FEASIBILITY STUDY ON ANOTHER APPLICATION OF PHASE TRANSITION MATERIALS

As well as thermal excitation, the phase transition is induced by the electric field, magnetic field, electron injection, photonic excitation, or strain. This chapter presents other applications of a phase transition material using its electrically-triggered phase transition. Before introducing the device examples, the properties of $VO_2$ contacts on top of the silicon substrate are analyzed. A MOSFET with a $VO_2$ thin film on the drain node is discussed here. The conceptual proposition and pristine electrical data are reviewed.

## *7.1 Analysis of Contacts between VO2 and Silicon*

The properties of $VO_2$ contacts formed on top of silicon are analyzed with the band theory. Figure 7.1 shows the band diagrams of n and p-type silicon, and metallic and insulating $VO_2$. The work functions are ~5.02 eV for p-type silicon with 1 x $10^{17}$ $cm^{-3}$ doping density, ~4.26 eV for n-type silicon with 1e16 $cm^{-3}$, ~5.15 eV for insulation $VO_2$ and ~5.30 eV for metallic $VO_2$. A few different values of work function of the $VO_2$ film have been reported using the different measurement tools [100]–[102]. Among them, the most recent result acquired from Kelvin Force

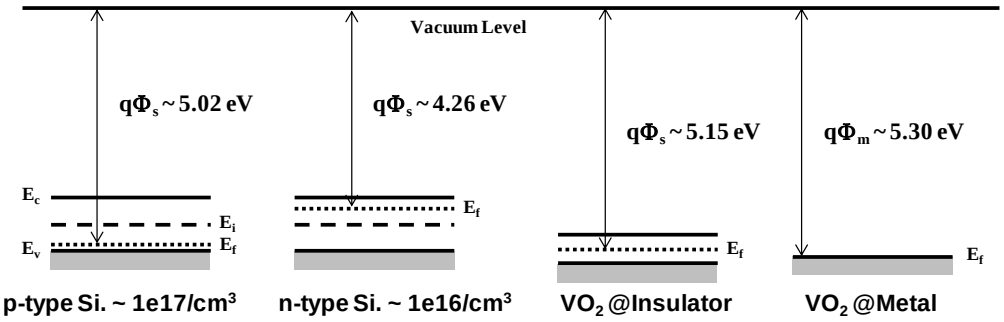



**Figure 7.1** Band diagrams of n or p-type silicon and metallic or insulating $VO_2$.

Microscopy (KRM) is selected in this chapter.

Figure 7.2 shows the energy band diagrams of contacts between $VO_2$ and silicon. In the metallic phase, when the contact is formed on the p-type silicon, it becomes ohmic as shown in Figure 7.2 (a). Whereas it is formed on the n-type silicon,

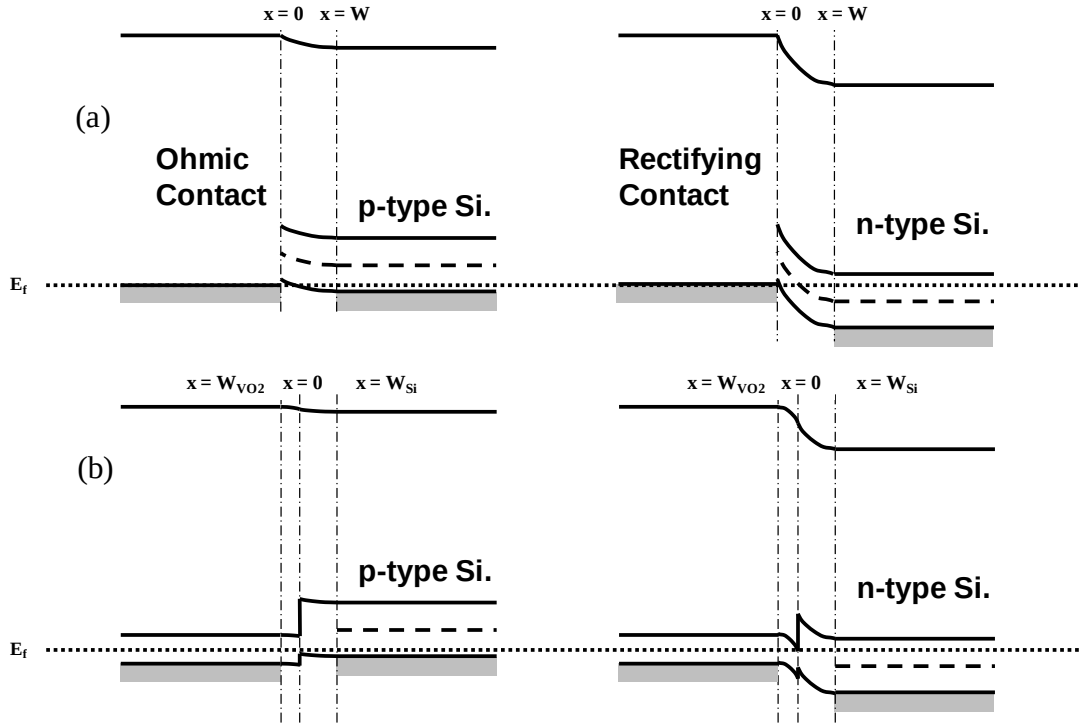



**Figure 7.2** Energy Band diagrams of contacts between $VO_2$ and the silicon: $VO_2$ is in the (a) metallic phase or (b) insulating phase.

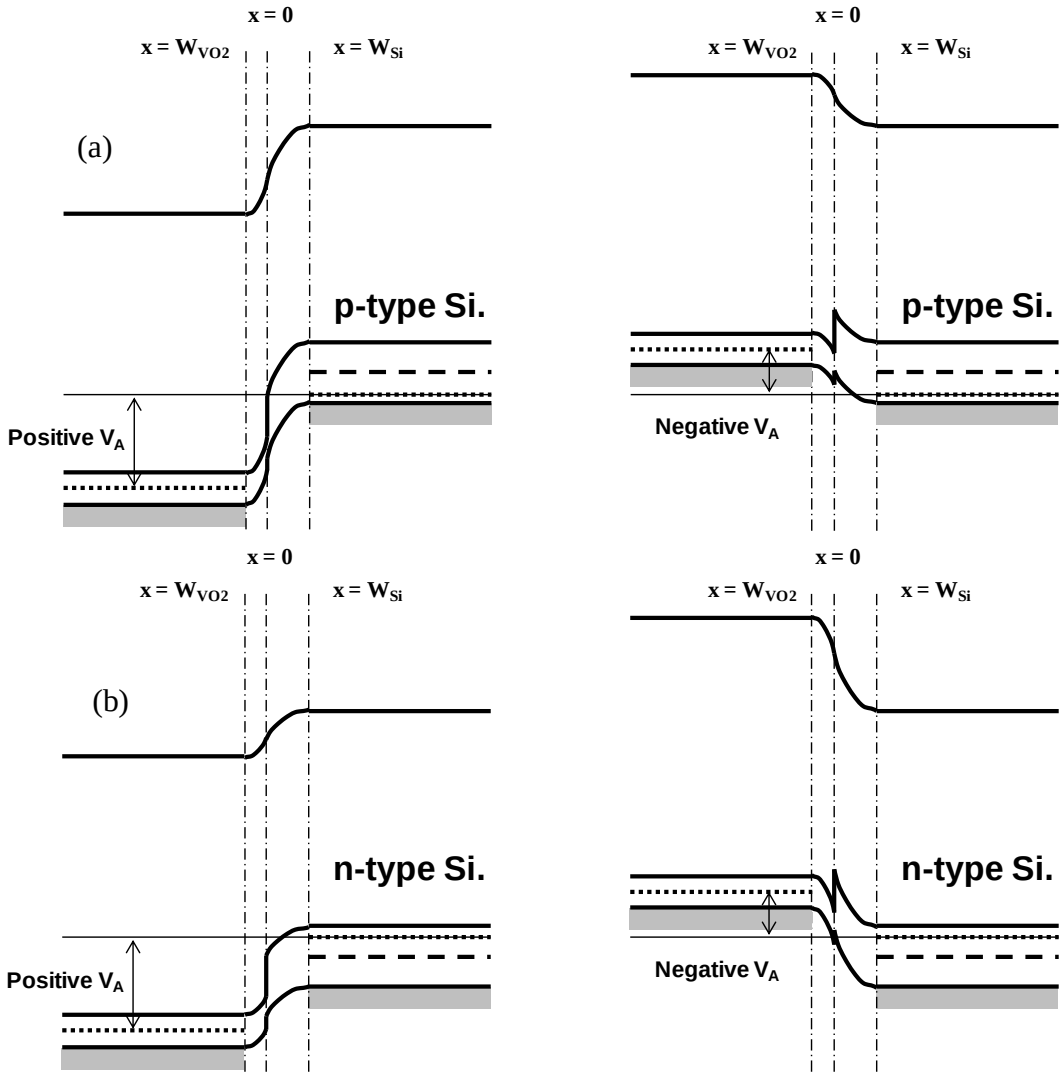



**Figure 7.3** Changes of the band energies of contacts between insulating $VO_2$ and the silicon at the applied voltage: $VO_2$ contact is formed on the (a) p-type silicon or (b) n-type silicon.

it becomes rectifying. Its schottky barrier is 1.04 eV. In the insulating phase, a type-II heterojunction is made at the interface between two layers. The change of the energy band at the applied voltage is shown in Figure 7.3. The change of depletion width according to the bias is ignored in the figure for simplicity. In case of the p-type silicon, forward bias condition is accomplished by the negative voltage applied at $VO_2$

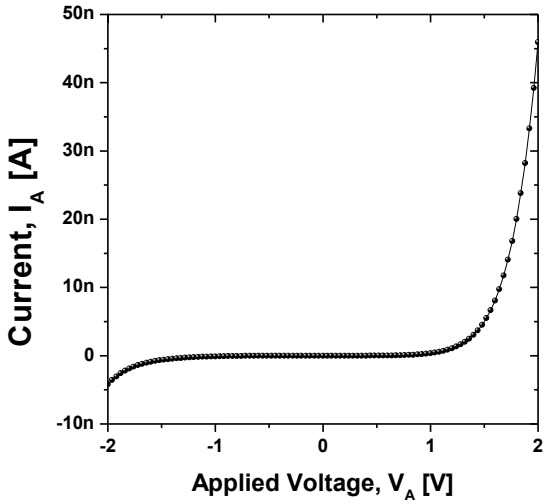



**Figure 7.4** Current vs. voltage plot of the heterojunction between an insulating $VO_2$ and an n+ doped silicon.

contact. At the reverse bias condition, this structure seems to be vulnerable to band to band tunneling. In case of the n-type silicon, forward bias condition is accomplished by the positive voltage applied at $VO_2$ contact. This structure has a 2-dimensional electron gas (2DEG), which is a gas of electrons confined to a triangular quantum well at the $VO_2$-silicon interface and moving freely to move in two dimensions. High-electron-mobility-transistors (HEMTs) utilize the 2DEG to get higher mobility than those in MOSFETs [103]. At the reverse bias condition, this structure seems to be vulnerable to electron tunneling from the 2DEG to the silicon. Figure 7.4 shows IV characteristics of the heterojunction between an insulating $VO_2$ and an n+ doped silicon. This result is well matched with the expectation from the analysis of band diagram.

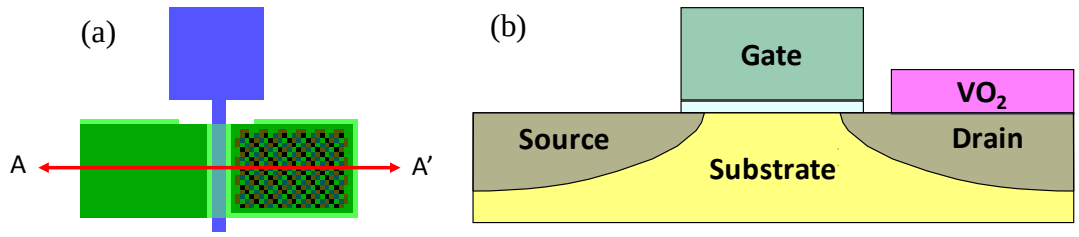



**Figure 7.5** Schematic views of the proposed transistor with a $VO_2$ film on the drain node: (a) top view and (b) A-A' cross section view.

## *7.2 MOSFET with a $VO_2$ Film on the Drain Node*

As discussed in Chapter 3, $VO_2$ has a current induced phase transition property. The phase transition of $VO_2$ occurs at the high current injection state even at room temperature as shown in Figure 3.5. Using this effect, a new transistor scheme is proposed. Figure 7.5 shows the schematic views of the proposed device. A $VO_2$ film is placed on the drain node. The resistivity of the metallic $VO_2$ is ~0.001 Ω·cm that is comparable to that of the silicon in the S/D region with the doping density of 1 x $10^{20}$ $cm^{-3}$. In the insulating phase of $VO_2$, its resistivity increases by more than 2 orders of

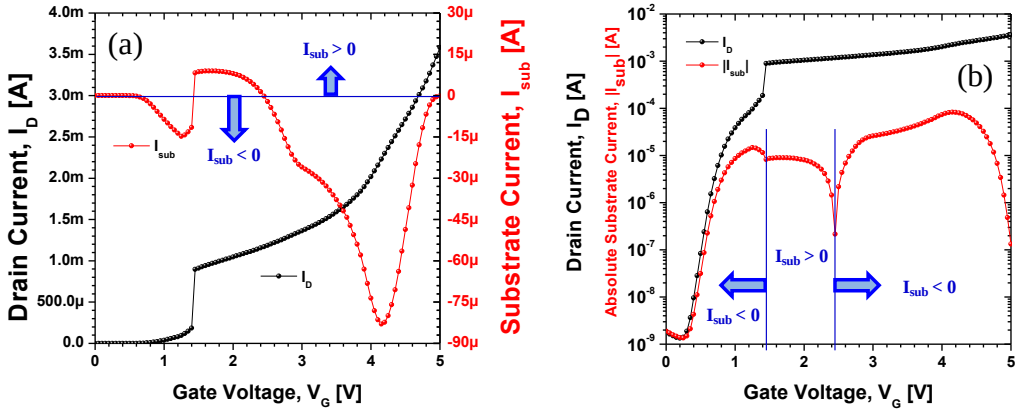



**Figure 7.6** Measured Drain and substrate currents in response to the gate voltage: (a) linear scale plot and (b) log scale one.

magnitude and thus the drain node has a high resistance state. That is, the actual drain voltage involved with the MOSFET operation is lower than the applied drain voltage due to the voltage drop caused by the resistance of $VO_2$. When the drain current reaches a critical current density to bring up the phase transition of $VO_2$, the drain node will have a low resistance state and hence the drain current will increase abruptly. Figure 7.6 shows the IV characteristics of the proposed device. The drain current exhibits a transition behavior corresponding to the expectation. The substrate current, however, shows an abnormal behavior and has a strong correlation to the drain current unexpectedly. At the transition point, the polarity of the substrate current changes from negative to positive and then decreases. After the transition, the substrate current has another transition point at around 4 V. This is a very strange phenomenon in a MOSFET operation. For now, to figure out this effect, more study and experiments are needed.

## *7.3 Summary*

The properties of $VO_2$-silicon contacts have been analyzed using the energy band diagrams. In the metallic state, $VO_2$ contacts are ohmic on the p-type silicon and rectifying on the n-type silicon. In the insulation phase, a type-II heterojunction is formed at the interface between two layers and the forward bias conditions are established by the negative $VO_2$ voltage on the p-type silicon and the positive $VO_2$ voltage on the n-type silicon. A MOSFET with a $VO_2$ thin film on the drain node has been proposed using the electrically-driven phase transition. The concept of the

application has been verified by a pristine experimental result, but additional experiments and study are needed.

# Chapter 8

# CONCLUSION

A new memory composed of a single element of transistor has been proposed. A phase transition thin film is inserted in between silicon dioxide layers and used as a gate insulator. Joule heating induced by current flowing through the channel is implemented for device operations. Through the thermal simulation, it has been confirmed that thermal energy delivered to the phase transition material is high enough to cause the phase transition of the material on top of the bottom oxide layer, but polarization switching effect dominated over the phase transition effect in the experiments. A thermal conduction equation was established for the calculation of switching energy and time of the proposed phase transition memory and the Joule heat of ~40 fJ and switching time of ~4 ns are estimated, which are superior or compatible to those of other memories.

$VO_2$, GST and SNO films were employed because these materials go through structural phase transition with the increase of temperature and their physical properties, such as resistance, reflectance and permittivity, change drastically. A conventional memory technology is employed for the fabrication and an i-line photolithography tool is adopted for photo-patterning. Bulk-type devices were made with p-type silicon wafers and suspended channel devices with p-type SOI wafers. To improve the heat delivery efficiency, a suspended channel phase transition memory with an air-gap under the channel has been proposed. Pyramidal and radial heat conduction models were established to calculate the heat transfer efficiency. The heat

transfer efficiency is 1.1 ~ 1.9% for the bulk-type device, 9.4 ~ 16.9% for the SOI device and 79 ~ 88.1% for the suspended channel device.

Irrespective of phase transition materials and device structures, the counterclockwise voltage hysteresis of gate capacitance was observed in response to gate voltage and consistent with the polarization switching effect. In case of $VO_2$ and GST, ferroelectric polarizations are dominant. On the other hand, space charge polarization is dominant in a SNO film. In $VO_2$ bulk devices, memory window of ~1 V was obtained in -4 to 4 V gate voltage cycling. Its remnant polarization of ~0.53 $\mu C/cm^2$ and coercive field of ~450 kV/cm were extracted from the saturation behavior of threshold voltage shift. Similar to other ferroelectric memory structures, depolarization effects are observed. The state of memory devices decayed gradually and retention times of approximately 15 minutes were observed at room temperature. Assuming the second order ferroelectric phase transition, the Curie-Weiss temperature of $VO_2$ was extrapolated from the correlation plot of memory window versus temperature and its value is around 450 K. At lower temperatures, the polarization of $VO_2$ disappears exponentially. It is believed that the origin for the low temperature effect of polarization may arise from the freezing of switchable polarization. In GST suspended channel devices, hysteresis memory window of ~1 V under ±4 V cycling and retention times of hundreds of seconds were observed. Extracted remnant polarization was ~0.13 $\mu C/cm^2$. The degradation of the polarization was also observed at low temperature and this is likely to result from charge trapping effect as well as the freezing of switchable polarization. In SNO bulk devices, the response time of polarization is above 1 μs, which implies that space charge polarization is likely

dominant in the permittivity of SNO. Hysteretic behaviors of SNO devices can be explained by Poole-Frenkel charge trapping/detrapping mechanism.

While the devices are volatile due to depolarization field, they hold some attraction as embedded single element DRAMs because of their simplicity. These results contribute to the emerging field of correlated oxide electronics and their integration with silicon platforms. This memory structure operates at very low voltages and thus is expected to be a good candidate for a variety of memory applications.

# Appendix

# 1. DETAILS ON THE FABRICATION PROCESS OF A BULK-TYPE PHASE TRANSITION DEVICE

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| A0010 | 0.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| A0020 | 0.0_MOS CLN_QDR1 | Res. > 16MΩ | | |
| A0030 | 0.0_MOS CLN_Acid Bath | 10 min. | | |
| A0040 | 0.0_MOS CLN_QDR2 | Res. > 16MΩ | | |
| A0050 | 0.0_MOS CLN_HF Dip | 30 sec. | | |
| A0060 | 0.0_MOS CLN_QDR3 | Res. > 16MΩ | | |
| A0070 | 0.0_Spin Rinse_Pad Oxide | | | |
| A0080 | 0.0_Pad Ox. Growth | Dry oxidation with HCI<br>900 °C, 40 min. | | TCA furnace |
| **0.5 Key Generation** | | | | |
| A0090 | 0.5_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0100 | 0.5_Prebake | 95 °C, 1 min. | | Hotplate |
| A0110 | 0.5_Expose | ET = 0.30 sec | | AS200 |
| A0120 | 0.5_Post-expose Bake | 115 °C, 1 min. | | Hotplate |
| A0130 | 0.5_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| A0140 | 0.5_Descum | PR 10 nm Target | Oxygen CLN | Oxford 82 |
| A0150 | 0.5_Oxide Etch | $SiO_2$ 30 nm Target | $CHF_3/O_2$ | Oxford 82 |
| A0160 | 0.5_Si Etch | Si 1.5 μm Target | $SF_6/O_2$ | Oxford 82 |
| A0170 | 0.5_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| A0180 | 0.5_Spin Rinse_PR Strip | | | |
| A0190 | 0.5_MOS CLN_Base Bath | 10 min. | | MOS hood |
| A0200 | 0.5_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| A0210 | 0.5_MOS CLN_Acid Bath | 10 min. | | |
| A0220 | 0.5_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| A0230 | 0.5_Spin Rinse_Nitride | | | |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| A0240 | 0.5_Nitride Depo | Standard Nitride<br>775 °C, 30 min. | | TCA furnace |
| **1.0 Active** | | | | |
| A0250 | 1.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0260 | 1.0_Prebake | 95 °C, 1 min. | | Hotplate |
| A0270 | 1.0_Expose | ET = 0.24 sec. | | AS200 |
| A0280 | 1.0_Post-expose Bake | 115 °C, 1 min. | | Hotplate |
| A0290 | 1.0_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| A0300 | 1.0_Descum | PR 10 nm Target | Oxygen CLN | Oxford 82 |
| A0310 | 1.0_Nitride Etch | Nitride 120 nm Target | $SF_6/O_2$ | Oxford 82 |
| A0320 | 1.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| A0330 | 1.0 Spin Rinse_PR Strip | | | |
| A0340 | 1.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| A0350 | 1.0_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| A0360 | 1.0_MOS CLN_Acid Bath | 10 min. | | |
| A0370 | 1.0_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| A0380 | 1.0_Spin Rinse_Field Oxide | | | |
| A0390 | 1.0_Field Oxidation. | Wet oxidation with HCl<br>1100 °C, 45 min. | | TCA furnace |
| A0400 | 1.0_Oxide Etch_BOE | 6:1 BOE, 20 sec. | | Chemical Hood |
| A0410 | 1.0_$H_3PO_4$ Strip | 85% $H_3PO_4$, 160 °C<br>Nitride Target 120 nm | | Hot Phos. Hood |
| A0420 | 1.0_Spin Rinse_$H_3PO_4$ Strip | | | Hot Phos. Hood |
| A0430 | 1.0_Channel IIP | B, 40 KeV, 2e12 $cm^{-2}$,<br>Tilt 7°, Default Rotation | | Eaton implantor, performed by staff |
| **2.0 N+ SD IIP** | | | | |
| A0440 | 2.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0450 | 2.0_Prebake | 95 °C, 1 min. | | Hotplate |
| A0460 | 2.0_Expose | ET = 0.30 sec. | | AS200 |
| A0470 | 2.0_Post-expose Bake | 115 °C, 1 min. | | Hotplate |
| A0480 | 2.0_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| A0490 | 2.0_N+ SD IIP | As, 30 KeV, 3e15 $cm^{-2}$,<br>Tilt 0°, Default Rotation | | Eaton implantor, performed by staff |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| A0510 | 2.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| A0520 | 2.0_Spin Rinse_PR Strip | | | |
| A0530 | 2.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| A0540 | 2.0_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| A0550 | 2.0_MOS CLN_Acid Bath | 10 min. | | |
| A0560 | 2.0_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| A0570 | 2.0_Spin Rinse_RTA | | | |
| A0580 | 2.0_RTA | 1000 ℃, 10 sec. | | RTA08 |
| A0590 | 2.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| A0600 | 2.0_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| A0610 | 2.0_MOS CLN_Acid Bath | 10 min. | | |
| A0620 | 2.0_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| A0630 | 2.0_MOS CLN_HF Dip | 15 sec. | | |
| A0640 | 2.0_MOS CLN_QDR3 | Res. > 16 MΩ | | |
| A0650 | 2.0_Botton Oxide Growth | Dry oxidation with HCI<br>1000 ℃, 10 min. | | Oxide Tube |
| A0660 | 2.0_MIT Material Depo. | VO2 200 nm<br>GST 150 nm<br>SNO 200 nm | | Harvard<br>ETRI<br>Harvard |
| A0670 | 2.0_Top Oxide Depo. | Plasma 110 ℃,<br>500 cycles | | ALD |
| **3.0 Gate Insulator** | | | | |
| A0680 | 3.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0690 | 3.0_Prebake | 95 ℃, 1 min. | | Hotplate |
| A0700 | 3.0_Expose | ET = 0.24 sec. | | Stepper |
| A0710 | 3.0_Post-expose Bake | 115 ℃, 1 min. | | Hotplate |
| A0720 | 3.0_Development | AZ 726MIF, 2 min. | | Chemical Hood |
| A0730 | 3.0_Descum. | PR 10 nm Target | | Oxford 82 |
| A0740 | 3.0_Gate Insulator Etch | SiO2 60 nm Target<br>VO2 250 nm Target | CHF3/O2<br>$CF_4$ | Oxford 82 |
| | | SiO2 60 nm Target<br>GST 200 nm Target | $CHF_3/O_2$ | Oxford 82 |
| | | SiO2 60 nm Target<br>SNO 250 nm Target | $CHF_3/O_2$<br>Tilt 10° | Oxford 82<br>Vecco Ion Miller |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| A0750 | 3.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| A0760 | 3.0 Spin Rinse_PR Strip | | | |
| **4.0 Gate Metal** | | | | |
| A0770 | 4.0_LOR Coating | LOR process<br>3000 rpm, 45 sec.<br>LOR 5A | | Spinner |
| A0780 | 4.0_LOR Prebake | 180 °C, 5 min. | | Hotplate |
| A0790 | 4.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0800 | 4.0_Prebake | 95 °C, 1 min. 10 sec. | | Hotplate |
| A0810 | 4.0_Expose | ET = 0.24 sec. | | Stepper |
| A0820 | 4.0_Post-expose Bake | 115 °C, 1 min. 30 sec. | | Hotplate |
| A0830 | 4.0_Development | AZ 726MIF, 3 min. | | Chemical Hood |
| A0840 | 4.0_Descum. | PR 10 nm Target | | Oxford 82 |
| A0850 | 4.0_Metal Depo. | Ti 50 nm / Al 300 nm | | SC4500 Evap. |
| A0860 | 4.0_Lift-off | 1165, 1 day | | Chemical Hood |
| **5.0 S/D Metal** | | | | |
| A0870 | 5.0_LOR Coating | LOR process<br>3000 rpm, 45 sec.<br>LOR 5A | | Spinner |
| A0880 | 5.0_LOR Prebake | 180 °C, 5 min. | | Hotplate |
| A0890 | 5.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| A0900 | 5.0_Prebake | 95 °C, 1 min. 10 sec. | | Hotplate |
| A0910 | 5.0_Expose | ET = 0.24 sec. | | Stepper |
| A0920 | 5.0_Post-expose Bake | 115 °C, 1 min. 30 sec. | | Hotplate |
| A0930 | 5.0_Development | AZ 726MIF, 3 min. | | Chemical Hood |
| A0940 | 5.0_Descum. | PR 10 nm Target | | Oxford 82 |
| A0950 | 5.0_Oxide Etch_BOE | BOE 6:1, 2 min. | | Chemical Hood |
| A0960 | 5.0_Metal Depo. | Ti 50 nm / Al 300 nm | | SC4500 Evap. |
| A0970 | 5.0_Lift-off | 1165, 1 day | | Chemical Hood |
| A0980 | 5.0_Backside Etch_BOE | BOE 6:1 | | Chemical Hood |
| A0990 | 5.0_Metal Depo. | Ti 50 nm / Au 100 nm | | SC4500 Evap. |
| A1000 | 5.0_Passivation Alloy | 5% H2/Ar, 300 °C, 1 hr | | Anneal 3 |

# 2. DETAILS ON THE FABRICATION PROCESS OF A SUSPENDED CHANNEL PHASE TRANSITION DEVICE

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| B0010 | 0.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| B0020 | 0.0_MOS CLN_QDR1 | Res. > 16MΩ | | |
| B0030 | 0.0_MOS CLN_Acid Bath | 10 min. | | |
| B0040 | 0.0_MOS CLN_QDR2 | Res. > 16MΩ | | |
| B0050 | 0.0_MOS CLN_HF Dip | 30 sec. | | |
| B0060 | 0.0_MOS CLN_QDR3 | Res. > 16MΩ | | |
| B0070 | 0.0_Spin Rinse_Pad Oxide | | | |
| B0080 | 0.0_Pad Ox. Growth | Dry oxidation with HCI<br>900 °C, 40 min. | | TCA furnace |
| **0.5 Key Generation** | | | | |
| B0090 | 0.5_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0100 | 0.5_Prebake | 95 °C, 1 min. | | Hotplate |
| B0110 | 0.5_Expose | ET = 0.30 sec | | AS200 |
| B0120 | 0.5_Post-expose Bake | 115 °C, 1 min | | Hotplate |
| B0130 | 0.5_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| B0140 | 0.5_Descum | PR 10 nm Target | Oxygen CLN | Oxford 82 |
| B0150 | 0.5_Oxide Etch | $SiO_2$ 30 nm Target | $CHF_3/O_2$ | Oxford 82 |
| B0160 | 0.5_Si Etch | Si 450 nm Target | $SF_6/O_2$ | Oxford 82 |
| B0170 | 0.5_Oxide Etch | $SiO_2$ 500 nm Target | $CHF_3/O_2$ | Oxford 82 |
| B0180 | 0.5_Si Etch | Si 600 m Target | $CF_4$ & $SF_6/O_2$ | Oxford 82 |
| B0190 | 0.5_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| B0200 | 0.5_Spin Rinse_PR Strip | | | |
| **0.7 N+ SD IIP** | | | | |
| B0210 | 0.7_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0220 | 0.7_Prebake | 95 °C, 1 min. | | Hotplate |
| B0230 | 0.7_Expose | ET = 0.30 sec. | | AS200 |
| B0240 | 0.7_Post-expose Bake | 115 °C, 1 min. | | Hotplate |
| B0250 | 0.7_Develop | AZ 726MIF, 2 min. | | Chemical Hood |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| B0260 | 0.7_N+ SD IIP | As, 25 KeV, 1e15 $cm^{-2}$, Tilt 0°, Default Rotation | | Eaton implantor, performed by staff |
| B0270 | 0.7_Ashing | PR 2.5 μm Target | | Aura 1000 |
| B0280 | 0.7_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| B0290 | 0.7_Spin Rinse_PR Strip | | | |
| B0300 | 0.7_MOS CLN_Base Bath | 10 min. | | MOS hood |
| B0310 | 0.7_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| B0320 | 0.7_MOS CLN_Acid Bath | 10 min. | | |
| B0330 | 0.7_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| B0340 | 0.7_Spin Rinse_RTA | | | |
| B0350 | 0.7_RTA | 1000 °C, 10sec | | RTA08 |
| **1.0 Active** | | | | |
| B0360 | 1.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0370 | 1.0_Prebake | 95 °C, 1 min. | | Hotplate |
| B0380 | 1.0_Expose | ET = 0.24 sec. | | AS200 |
| B0390 | 1.0_Post-expose Bake | 115 °C, 1 min. | | Hotplate |
| B0400 | 1.0_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| B0410 | 1.0_Descum | PR 10 nm Target | Oxygen CLN | Oxford 82 |
| B0420 | 1.0_Oxide Etch | $SiO_2$ 30 nm Target | $CHF_3/O_2$ | Oxford 82 |
| B0430 | 1.0_Si Etch | Si 450 nm Target | $SF_6/O_2$ | Oxford 82 |
| B0440 | 1.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| B0450 | 1.0 Spin Rinse_PR Strip | | | |
| B0460 | 1.0_Etch Stopper Depo. | Plasma 200 °C,<br>300 cycles | | ALD |
| B0470 | 1.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| B0480 | 1.0_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| B0490 | 1.0_MOS CLN_Acid Bath | 10 min. | | |
| B0500 | 1.0_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| B0510 | 1.0_Spin Rinse_Nitride | | | |
| B0520 | 1.0_Nitride Depo | Standard Nitride<br>775 °C, 40 min. | | TCA furnace |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| **2.0 Channel Open** | | | | |
| B0530 | 2.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0540 | 2.0_Prebake | 95 ℃, 1 min. | | Hotplate |
| B0550 | 2.0_Expose | ET = 0.30 sec. | | AS200 |
| B0560 | 2.0_Post-expose Bake | 115 ℃, 1 min. | | Hotplate |
| B0570 | 2.0_Develop | AZ 726MIF, 2 min. | | Chemical Hood |
| B0580 | 2.0_Nitride Etch | Nitride 200 nm Target | $SF_6/O_2$ | Oxford 82 |
| B0590 | 2.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| B0600 | 2.0_Spin Rinse_PR Strip | | | |
| B0610 | 2.0_Oxide Etch_HF 49% | HF 49%, 2 min. | | Chemical Hood |
| B0620 | 2.0_$H_3PO_4$ Strip | 85% $H_3PO_4$, 160 ℃<br>Nitride Target 200 nm | | Chemical Hood |
| B0630 | 2.0_Spin Rinse_$H_3PO_4$ Strip | | | Hot Phos. Hood |
| B0640 | 2.0_MOS CLN_Base Bath | 10 min. | | MOS hood |
| B0650 | 2.0_MOS CLN_QDR1 | Res. > 16 MΩ | | |
| B0660 | 2.0_MOS CLN_Acid Bath | 10 min. | | |
| B0670 | 2.0_MOS CLN_QDR2 | Res. > 16 MΩ | | |
| B0680 | 2.0_MOS CLN_HF Dip | 15 sec. | | |
| B0690 | 2.0_MOS CLN_QDR3 | Res. > 16 MΩ | | |
| B0700 | 2.0_Botton Oxide Growth | Dry oxidation with HCI<br>1000 ℃, 10 min. | | Oxide Tube |
| B0710 | 2.0_MIT Material Depo. | GST 150 nm | | ETRI |
| B0720 | 2.0_Top Oxide Depo. | Plasma 110 ℃,<br>500 cycles | | ALD |
| **3.0 Gate Insulator** | | | | |
| B0730 | 3.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0740 | 3.0_Prebake | 95 ℃, 1 min. | | Hotplate |
| B0750 | 3.0_Expose | ET = 0.24 sec. | | Stepper |
| B0760 | 3.0_Post-expose Bake | 115 ℃, 1 min. | | Hotplate |
| B0770 | 3.0_Development | AZ 726MIF, 2 min. | | Chemical Hood |
| B0780 | 3.0_Descum. | PR 10 nm Target | | Oxford 82 |
| B0790 | 3.0_Gate Insulator Etch | SiO2 60 nm Target<br>GST 200 nm Target | $CHF_3/O_2$ | Oxford 82 |

| Step # | Step Description | Step parameters | Recipe | Equipment |
|---|---|---|---|---|
| B0800 | 3.0_PR Strip | Bath 1, 10 min.<br>Bath 2, 15 min.<br>QDR | | PR Strip Hood |
| B0810 | 3.0 Spin Rinse_PR Strip | | | |
| **4.0 Gate Metal** | | | | |
| B0820 | 4.0_LOR Coating | LOR process<br>3000 rpm, 45 sec.<br>LOR 5A | | Spinner |
| B0830 | 4.0_LOR Prebake | 180 °C, 5 min. | | Hotplate |
| B0840 | 4.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0850 | 4.0_Prebake | 95 °C, 1 min. 10 sec. | | Hotplate |
| B0860 | 4.0_Expose | ET = 0.24 sec. | | Stepper |
| B0870 | 4.0_Post-expose Bake | 115 °C, 1 min. 30 sec. | | Hotplate |
| B0880 | 4.0_Development | AZ 726MIF, 3 min. | | Chemical Hood |
| B0890 | 4.0_Descum. | PR 10 nm Target | | Oxford 82 |
| B0900 | 4.0_Metal Depo. | Ti 50 nm / Al 600 nm | | SC4500 Evap. |
| B0910 | 4.0_Lift-off | 1165, 1 day | | Chemical Hood |
| **5.0 S/D Metal** | | | | |
| B0920 | 5.0_LOR Coating | LOR process<br>3000 rpm, 45 sec.<br>LOR 5A | | Spinner |
| B0930 | 5.0_LOR Prebake | 180 °C, 5 min. | | Hotplate |
| B0940 | 5.0_PR Coating | P20 Precoating<br>SPR 700-1.2<br>3000 rpm, 30 sec. | | Spinner |
| B0950 | 5.0_Prebake | 95 °C, 1 min. 10 sec. | | Hotplate |
| B0960 | 5.0_Expose | ET = 0.24 sec. | | Stepper |
| B0970 | 5.0_Post-expose Bake | 115 °C, 1 min. 30 sec. | | Hotplate |
| B0980 | 5.0_Development | AZ 726MIF, 3 min. | | Chemical Hood |
| B0990 | 5.0_Descum. | PR 10 nm Target | | Oxford 82 |
| B1000 | 5.0_Oxide Etch_BOE | BOE 6:1, 2 min. | | Chemical Hood |
| B1010 | 5.0_Metal Depo. | Ti 50 nm / Al 300 nm | | SC4500 Evap. |
| B1020 | 5.0_Lift-off | 1165, 1 day | | Chemical Hood |
| B1030 | 5.0_Backside Etch_BOE | BOE 6:1 | | Chemical Hood |
| B1040 | 5.0_Metal Depo. | Ti 50 nm / Au 100 nm | | SC4500 Evap. |

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